PXIe-9529

8-CH 24-Bit 192 kS/s
Dynamic Signal Acquisition Module

User's Manual

Manual Rev.: 2.00

Revision Date: Oct. 31, 2013

Part No: 50-17045-1000

Recycled Paper

Advance Technologies; Automate the World.

Revision History

Revision	Release Date	Description of Change(s)
2.00	Oct. 31, 2013	Initial Release

Preface

Copyright 2013 ADLINK Technology, Inc.

Disclaimer

The information in this document is subject to change without prior notice in order to improve reliability, design, and function and does not represent a commitment on the part of the manufacturer.

In no event will the manufacturer be liable for direct, indirect, special, incidental, or consequential damages arising out of the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Environmental Responsibility

ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE:

Additional information, aids, and tips that help users perform tasks.

CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

Table of Contents

List of Figures

This page intentionally left blank.

List of Tables

This page intentionally left blank.

1 Introduction

The PXIe-9529 is a high-performance 8-CH 24-Bit 192 kS/s dynamic signal acquisition module, specifically designed for applications such as structural health monitoring, noise, vibration, and harshness (NVH) measurement, and phased array data acquisition.

The PXIe-9529 features 24-bit simultaneous sampling at 192 kS/s over 8 channels, and a 110 dB dynamic range, providing ample power for high-density, high channel count signal measurement, and vibration-optimized lower AC cutoff frequency of 0.3 Hz. All input channels incorporate 4 mA bias current for integrated electronic piezoelectric (IEPE) signal conditioning for accelerometers and microphones.

The PXIe-9529 is auto-calibrated with an onboard reference circuit calibrating offset and acquiring analog input errors. Following auto-calibration, the calibration constant is stored in EEPROM, such that these values can be loaded and used as needed by the board. There is no requirement to calibrate the module manually.

1.1 Features

- PXI Express specification Rev. 1.0 compliant
- Up to 200 MS/s sampling rate
- 8 simultaneous analog inputs
- 192 kS/s maximum sampling rate
- AC or DC input coupling, software selectable
- Support for:
  - One external digital trigger input
  - IEPE output on each analog input, software configurable
  - Auto-calibration

1.2 Applications

- Structural health monitoring
- Phase array data acquisition
- Noise, vibration, and harshness (NVH) detection
- Machine status monitoring

1.3 Specifications

1.3.1 Analog Input

Channel Characteristics		Comment
Channels	8	
Type	Differential or Pseudo-Differential	
Coupling	AC or DC, software selectable	
AC coupling cutoff frequency	0.5Hz	
ADC resolution	24-Bit	
ADC type	Delta-sigma	
Input signal range	±10V, ±1V	
Sampling rate (fs)	8 kS/s to 192 kS/s, 768 µS/s increments for fs > 108 kS/s, 576 µS/s increments for 54 kS/s ≤ fs ≤108 kS/s	
Over voltage protection	Differential: ±42.4V, Pseudo-differential: ▶ positive terminal ±42.4 V ▶ negative terminal unprotected, rated at ±2.5 V	
Input impedance	1MΩ, (50Ω between negative input and system ground for pseudo-differential mode)	
Offset error	±1 mV max.	
Gain error	±0.1% of FSR	

Channel Characteristics		Comment
SNR, @fin = 1kHz	103 dB	fs = 8.0 kS
	104 dB	fs = 54.0 kS
	99 dB	fs = 108 kS
	98 dB	fs = 192 kS
THD	< -106 dB	
SFDR	> 106 dB	
crosstalk	< -100 dB	
-3 dB bandwidth	>0.4863 fs	fs < 108 kS
	≅ 0.2 fs	fs > 108 kS
IEPE		
Current	4 mA, each channel independently software configurable	
Compliance	24V	

Table 1-1: Channel Characteristics

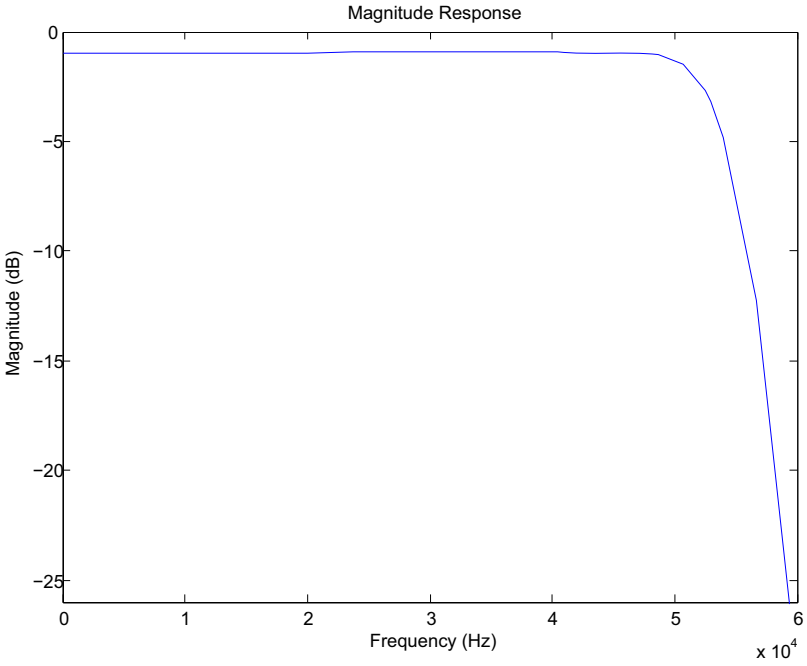


Figure 1-1: Analog Input Channel Bandwidth, ±0.2 Vpp

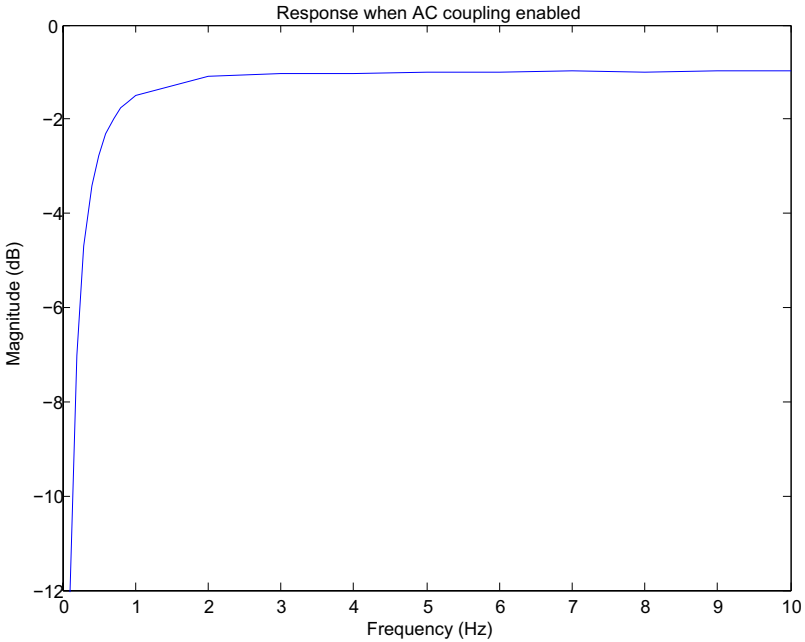


Figure 1-2: Analog Input Channel Bandwidth, ±2 Vpp

1.3.2 Timebase

Sampling Clock	
Timebase options	Internal: onboard synthesizer
	External: PXI_CLK10, PXIe_CLK100
Timebase accuracy	< ± 25ppm

Table 1-2: Timebase

1.3.3 Triggers

Trigger Source & Mode	
Trigger source	Software, external digital trigger, analog trigger, PXI trigger bus[0..7], PXI_STAR, and PXIe_DSTARB
Trigger mode	Post trigger and delay trigger

Table 1-3: Trigger Source & Mode

Digital Trigger Input	
Sources	Front panel SMA connector
Compatibility	3.3 V TTL, 5 V tolerant
Input high threshold	2.0 V
Input low threshold (VIL)	0.8 V
Maximum input overload	-0.5 V to +5.5 V
Trigger polarity	Rising or falling edge
Pulse width	20 ns minimum

Table 1-4: Digital Trigger Input

1.3.4 General Specifications

Physical	
Physical dimensions	160 W x 100 H mm (6.24 x 3.9 in)
Bus	
Bus interface	PCI Express Gen 1 x 4
Environmental Tolerance	
Operating	Temperature: 0°C - 55°C Relative humidity: 10% - 90%, non-condensing
Storage	Temperature: -20°C - +80°C Relative humidity: 10% - 90%, non-condensing

Calibration	
Onboard reference	+5.000 V

Calibration	
Temperature coefficient	< 5.0 ppm/°C
Warm-up time	15 minutes

Power Consumption		
Power Rail	**Standby Current (mA)**	**Full Load (mA)**
+3.3 V	102	102.2
+12 V	20	20
+5V	1920	2010

1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW®.

All software options are included in the ADLINK All-in-One CD. Commercial software drivers are protected with licensing codes. Without the code, you may install and run the demo version for trial/demonstration purposes for only up to two hours. Contact your ADLINK dealer to purchase the software license.

1.4.1 SDK

For customers who want to write their own programs, ADLINK provides the following software development kits.

- ▷ DAQPilot for Windows, compatible with various application environments, such as VB.NET, VC.NET, VB/VC++, BCB, and Delphi
- ▷ DAQPilot for LabVIEW
- ▷ Toolbox adapter for MATLAB

1.4.2 DSA-DASK

DSA-DASK includes device drivers and DLL for Windows XP/7/8. DLL is binary compatible across Windows XP/7/8. This

means all applications developed with DSA-DASK are compatible with these Windows operating systems. The development environment may be VB, VB.NET, VC++, BCB, and Delphi, or any Windows programming language that allows calls to a DLL. The DSA-DASK user and function reference manuals are on the ADLINK All-in-One CD.

1.5 Device Layout and I/O Array

NOTE:

All dimensions are in mm

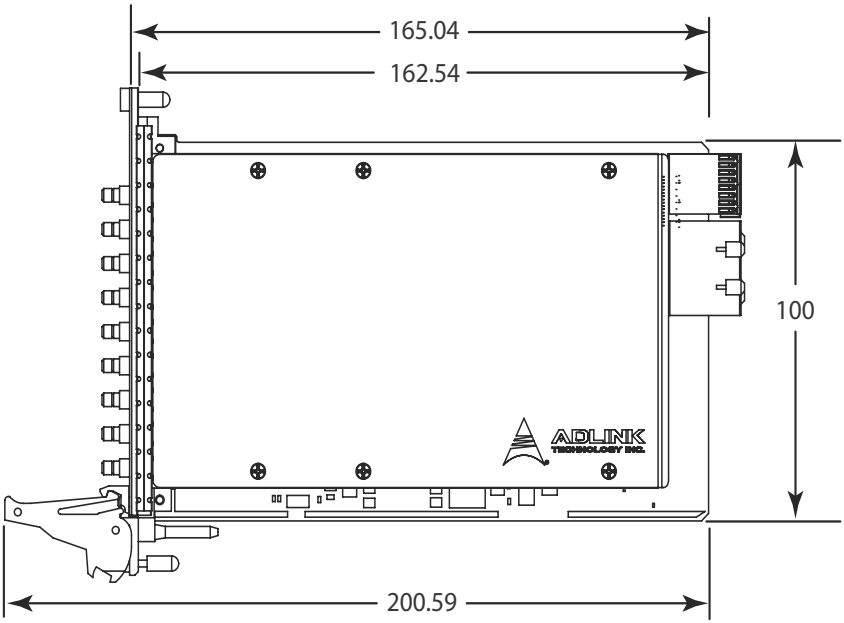


Figure 1-3: PXIe-9529 Schematic

The PXIe-9529 I/O array is labeled to indicate connectivity, as shown.

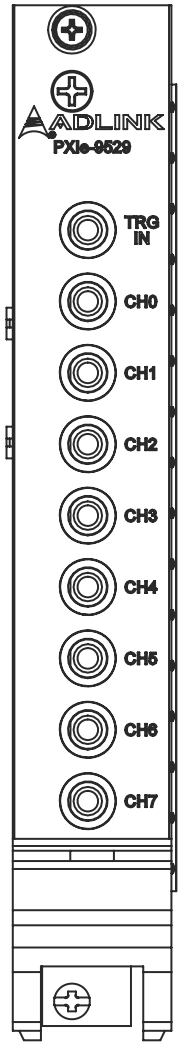


Figure 1-4: PXIe-9529 I/O Array

This page intentionally left blank.

2 Getting Started

This chapter describes proper installation environment, installation procedures, package contents and basic information users should be aware of regarding the PXIe-9529.

NOTE:

Diagrams and illustrated equipment are for reference only. Actual system configuration and specifications may vary.

2.1 Installation Environment

When unpacking and preparing to install, please refer to Important Safety Instructions.

Only install equipment in well-lit areas on flat, sturdy surfaces with access to basic tools such as flat- and cross-head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools

- Phillips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Antistatic mat

ADLINK PXIe-9529 DSA modules are electrostatically sensitive and can be easily damaged by static electricity. The module must be handled on a grounded anti-static mat. The operator must wear an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the carton and packaging for damage. Shipping and handling could cause damage to the equipment inside. Make sure that the equipment and its associated components have no damage before installation.

The equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing.

- **Package Contents**
- PXIe-9529 dynamic signal acquisition module
- ADLINK All-in-One compact disc
- PXIe-9529 Quick Start Guide

If any of these items are missing or damaged, contact the dealer

Do not install or apply power to equipment that is damaged or missing components. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/vendor immediately for assistance and obtain authorization before returning any product.

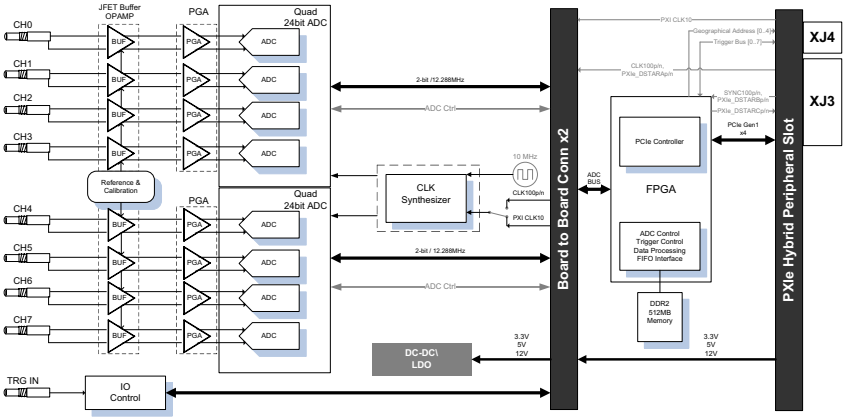
2.2 Installing the Module

1. Turn off the PXI system/chassis and disconnect the power cable from the power source.
2. Align the module edge with the module guide in the PXI chassis.
3. Slide the module into the chassis until resistance is felt from the PXI connector.
4. Push the ejector upwards and firmly seat the module into the chassis.
5. Once the module is fully seated, a “click” can be heard from the ejector latch.
6. Tighten the screw on the front panel.
7. Connect the power plug to a power source and turn on the PXI system/chassis.

3 Operations

This chapter contains information regarding analog input, triggering and timing for the PXIe-9529.

3.1 Functional Block Diagram



3.2 Analog Input Channel

3.2.1 Analog Input Front-End Configuration

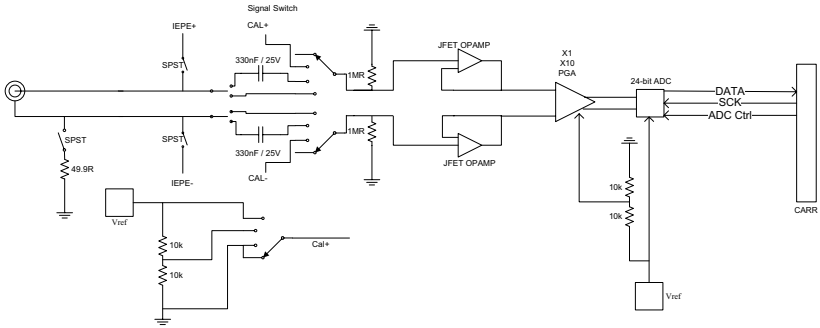


Figure 3-1: Analog Input Architecture

Differential and Pseudo-Differential Input Configuration

The PXIe-9529 provides both differential and psuedo-differential input configurations, with differential input mode providing voltage to the anode and cathode inputs of the SMB connector according to signal voltage difference therebetween. If the signal source is ground-referenced, differential input mode can be used for common-mode noise rejection.

If the signal source is a floating signal, pseudo-differential input mode can provide a reference ground connected to the cathode input of the SMB through a 50 Ω resistor, preventing the floating source from drifting over the input common-mode range.

Recommended configurations for the signal sources are as follows.

Signal Source Type	Card Configuration
Floating	Pseudo Differential
Ground-Reference	Differential

AC and DC Input Coupling

AC and DC coupling are available. With DC coupling, DC offset present in the input signal is passed to ADC, and is indicated if the signal source has a small level of offset voltage or if DC content of the signal is important. In AC coupling, the DC offset present in the input signal is erased, and is indicated if the DC content of the input signals is to be rejected. AC coupling enables a high pass R-C filter through the input signal path. The corner frequency (-3dB) is about 0.5Hz.

Input for IEPE

For applications that require sensors such as accelerometers or microphones, the PXIe-9529 provides an excitation current source. The common excitation current is usually about 4mA for these IEPE sensors. A DC voltage offset is generated due to the excitation current and sensor impedance. When IEPE current sources are enabled, the PXIe-9529 automatically sets input configuration to AC coupling.

3.2.2 Input Range and Data Format

When using an A/D converter, properties of the signal to be measured should be considered prior to selecting channel and signal connection to the module. A/D acquisition is initiated by a trigger source, which must be predetermined.Data acquisition commences once the trigger condition is established. Following completion of A/D conversion, A/D data is buffered in a Data FIFO, and can then be transferred to PC memory for further processing. Transfer characteristics of the two input ranges of the PXIe-9529 are as follows. Data format of the PXIe-9529 is 2's complement.

.

Description	Full-scale range	Least significant bit	FSR-1LSB	-FSR
Bipolar Analog Input	±10 V	1.19 μV	9.99999881 V	-10 V
	±1V	0.119 μV	0.999999881V	-1 V
Digital Code	N/A	N/A	7FFFFF	800000

Table 3-1: Input Range and Data Format

Description	Midscale +1LSB	Midscale	Midscale –1LSB
Bipolar Analog Input	1.19 μV	0 V	-1.19 μV
	0.119 μV	0 V	-0.119 μV
Digital Code	000001	000000	-FFFFFF

Table 3-2: Input Range Midscale Values

3.2.3 ADC and Analog Input Filter

ADC (Analog-to-Digital Converter)

The PXIe-9529 provides sigma-delta analog-to-digital converters, suitable for vibration, audio, and acoustic measurement. Analog side of the sigma-delta ADC is 1-bit, and the digital side performs oversampling, noise shaping and digital filtering. For example, if a desired sampling rate is 108kS/s, each ADC samples input signals

at 27.648MS/s, 256 times the sampling rate. The 1-bit 27.648MS/s data streams from 1-bit ADC to its internal digital filter circuit to produce 24-bit data at 108kS/s. The noise shaping removes quantization noise from low frequency to high frequency. At the last stage, the digital filter improves ADC resolution and removes high frequency quantization noise. The relationship between ADC sample rate and DDS output clock is as follows.

Sampling Rate	DDS(PLL) CLK
8k to 54kS/s	6.144M~41.472MHz
54K to 108kS/s	13.824 M to 27.648 MHz
108K to 192kS/s	20.736 M to 36.864 MHz

Table 3-3: ADC Sample Rates vs DDS Output Clock

Filter

Each channel has a two-pole lowpass filter. The filters limit bandwidth of the signal path and reject wideband noise.

3.2.4 DMA Data Transfer

The PXIe-9529, as a PCIe Gen1 X 4 device, provides a 192KS/s sampling rate ADC, generating a 3.072 MByte/second rate. To provide efficient data transfer, a PCI bus-mastering DMA is essential for continuous data streaming, as it helps to achieve the full potential PCI Express bus bandwidth. The bus-mastering controller releases the burden on the host CPU since data is directly transferred to the host memory without intervention. Once analog input operation begins, the DMA returns control of the program. During DMA transfer, the hardware temporarily stores acquired data in the onboard AD Data FIFO, and then transfers the data to a user-defined DMA buffer in the computer.

Using a high-level programming library for high speed DMA data acquisition, the sampling period and the number of conversions needs simply to be assigned into specified counters. After the AD trigger condition is met, the data will be transferred to the system memory by the bus-mastering DMA. In a multi-user or multi-task-

ing OS, such as Microsoft Windows, Linux, or other, it is difficult to allocate a large continuous memory block. Therefore, the bus controller provides DMA transfer with

scatter-gather function to link non-contiguous memory blocks into a linked list to enable transfer of large amounts of data without memory limitations. In non-scatter-gather mode, the maximum DMA data transfer size is 2 MB double words (8 MB bytes); in scatter-gather mode, there is no limitation on DMA data transfer size except the physical storage capacity of the system. Users can also link descriptor nodes circularly to achieve a multibuffered DMA. A linked list comprising three DMA descriptors. Each descriptor contains a PCI address, PCI dual address, a transfer size, and the pointer to the next descriptor.PCI address and PCI dual address support 64-bit addresses which can be mapped into more than 4 GB of address space, as shown.

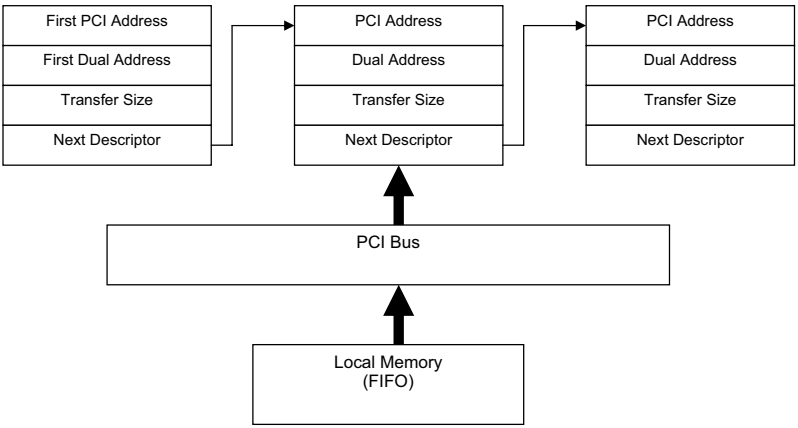


Figure 3-2: Linked List of PCI Address DMA Descriptors

3.3 Trigger Source and Trigger Modes

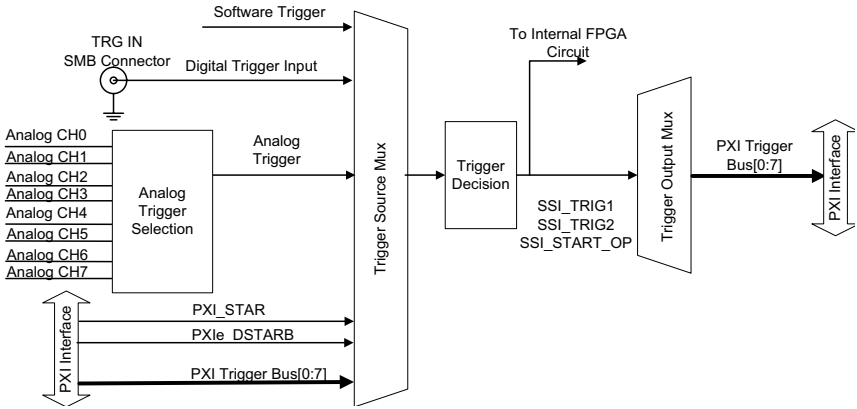


Figure 3-3: Trigger Architecture

The PXIe-9529 requires a trigger to implement acquisition of data. Configuration of triggers requires identification of trigger source. The PXIe-9529 supports internal software trigger, external digital trigger, PXI_STAR trigger, PXIe_DSTARB, PXI Trigger Bus [0.7], and SSI bus as well as analog trigger.

Software Trigger

The software trigger, generated by software command, is asserted immediately following execution of specified function calls to begin the operation.

External Digital Trigger

An external digital trigger is generated when a TTL rising edge or a falling edge is detected at the SMB connector on the front panel. As shown, trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL compatible, with minimum pulse width 10ns.

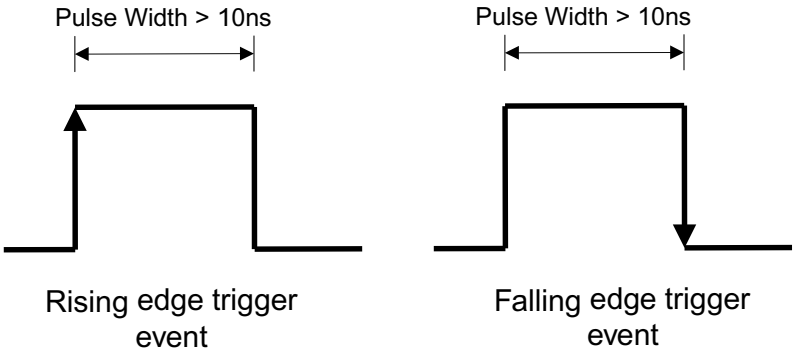


Figure 3-4: External Digital Trigger

PXI STAR Trigger

When PXI STAR is selected as the trigger source, the PXIe-9529 accepts a TTL-compatible digital signal as a trigger signal. The trigger occurs when a rising edge or falling edge is detected at PXI STAR, with trigger polarity configurable by software, with minimum pulse width requirement of the digital trigger signal 300 ns.

PXIe_DSTARB Trigger

The PXIe_DSTARB signal, a differential signal transmitted via the PXI Express Chassis backplane, distributes high-speed, high-quality trigger signals. When PXIe_DSTARB is selected as the trigger source, the PXIe-9529 accepts a fast-switching LVDS digital signal as a trigger signal. Triggering occurs when a rising edge or falling edge is detected at PXIe_DSTARB, with trigger polarity configurable by software, with minimum pulse width requirement 300 ns.

PXI Trigger Bus

The PXIe-9529 utilizes PXI Trigger Bus Numbers 0 through 7 to act as a System Synchronization Interface (SSI). With the interconnected bus provided by PXI Trigger Bus, multiple modules are easily synced. When configured as input, the PXIe-9529 serves as a slave module and can accept trigger

signals from one of buses 0 through 7. When configured as output, the PXIe-9529 serves as a master module and can output trigger signals to the PXI Trigger Bus Numbers 0 through 7.

Analog Trigger

The PXIe-9529 analog trigger circuitry can be configured to monitor one analog input channel from which data is acquired. Selection of an analog input channel as the analog trigger channel does not influence the input channel acquisition operation. The analog trigger circuit generates an internal digital trigger signal based on the condition between the analog signal and the defined trigger level.

Analog trigger conditions are as follows:

- ▷ Positive-slope trigger: The trigger event occurs when the analog input signal changes from a voltage lower than the specified trigger level to a voltage exceeding the specified trigger level.
- ▷ Negative-slope trigger: The trigger event occurs when the analog input signal changes from a voltage exceeding the specified trigger level to a voltage lower than the specified trigger level.

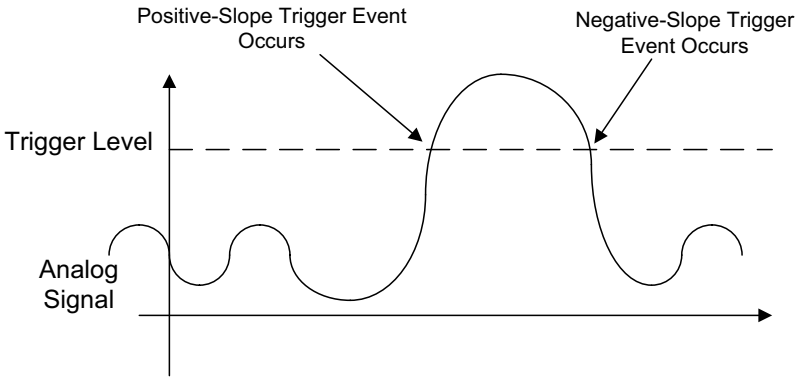


Figure 3-5: Analog Trigger Conditions

Trigger signal can be chosen from among CH0, CH1, CH2,CH3, CH4, CH5, CH6 and CH7 during use of an external

analog trigger source. The trigger level can be set by software with 24-bit resolution, with characteristics as shown.

Trigger Level Setting (Hex)	Trigger Voltage (-10V to +10V Range)	Trigger Voltage (-1V to +1V Range)
7FFFFF	9.99999881 V	0.999999881 V
7FFFFE	9.99999762 V	0.999999762 V
1	1.19 μV	0.119 μV
0	0V	0V
FFFFFF	-1.19 μV	-0.119 μV
800001	-9.99999881 V	-0.999999881 V
800000	-10 V	-1 V

Table 3-4: Preferred Characteristics for Analog Triggers

Trigger Export

The PXIe-9529 can export trigger signals to PXI Trigger Bus Numbers 0 through 7, utilizing them to act as the System Synchronization Interface. When configured as the output, the PXIe-9529 serves as a master module and can output trigger signals to synchronize the slave modules, with the trigger signal routed to any of the seven PXI Trigger Bus Numbers via software.

3.4 Trigger Mode

Two trigger modes applied to trigger sources initiate different data acquisition timings when a trigger event occurs, as applied to analog input and output functions.

Post Trigger Mode

If post trigger mode is configured, activity commences once the following trigger conditions are met:

- ▷ The analog input channel acquires a programmed number of samples at a specified sampling rate
- ▷ The analog output channel outputs pre-defined voltage at a specified output rate

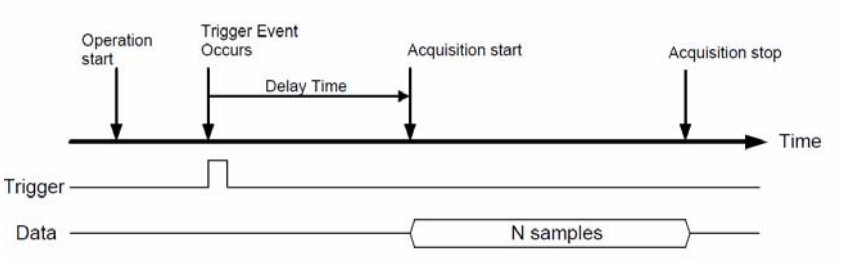


Figure 3-6: Post-Trigger Acquisition

Delay Trigger Mode

If delay trigger mode is configured, delay time from when the trigger event asserts to the beginning of the acquisition and waveform generation can be specified, as shown. Delay time is specified by a 32-bit counter value with the counter clocking based on the PCIe clock. Accordingly, maximum delay time is the period of PCIe_CLK X (2^32 - 1) and minimum is the period of PCIe_CLK (8 ns).

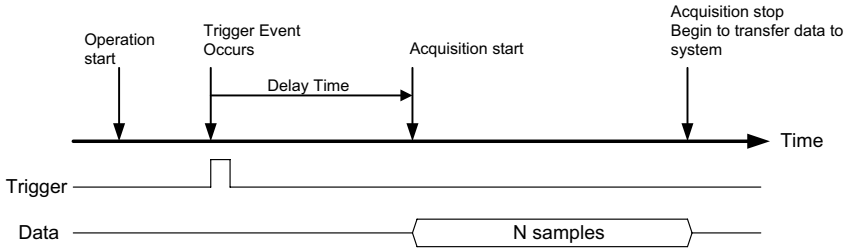


Figure 3-7: Delay Trigger Mode Acquisition

Post-Trigger or Delay-Trigger Acquisition with Re-Trigger

Post-trigger or delay trigger acquisition with re-trigger function enables collection of data after several trigger events, as shown. When the number of triggers is defined, the PXIe-9529 acquires specific sample data each time a trigger is accepted. All sampled data is stored in onboard memory first, until all trigger events have occurred, such that time between the previous sampled data and the subsequent trigger event can be only

one clock period of PCIe CLK. After the initial setup, no additional software intervention is required.

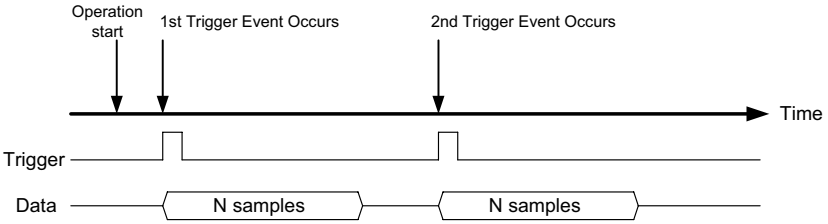


Figure 3-8: Re-Trigger Mode Acquisition

3.5 ADC Timing Control

3.5.1 Timebase

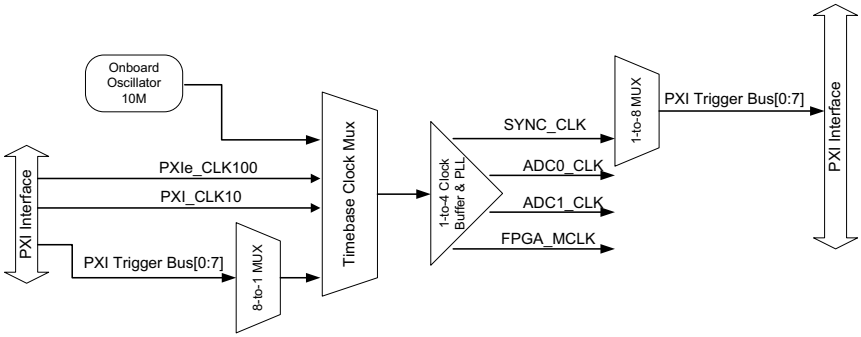


Figure 3-9: Timebase Architecture

An onboard timebase clock drives the sigma-delta ADC, with frequency exceeding the sample rate and produced by a PLL chip, with output frequency programmable to superior resolution. The PXIe- 9529 accepts the external 10MHz and 100MHz clocks from the PXI Express backplane for improved synchronization between modules.

3.5.2 DDS Timing vs. ADC

Sampling Rate	8k – 54kS/s	54k - 108kS/s	108 k – 192kS/s
DDS(PLL) CLK	6.144 M-41.472 MHz	13.824 M-27.648 MHz	20.736 M-36.864 MHz

Table 3-5: Timing Relationship between ADC and PLL Clock

3.5.3 Filter Delay in ADC

Filter delay indicates time required for data propagation through a converter. Both AI channels experience filter delay due to filter circuitry and converter architecture, as shown.

Update Rate (kS/s)	Filter Delay (samples)
8 K - 54 kS/s	13
54 K - 108 kS/s	13
108 K-192 kS/s	5

Table 3-6: ADC Filter Delay

3.6 Synchronizing Multiple Modules

The SSI (System Synchronization Interface) provides DAQ timing synchronization between multiple cards, with a bidirectional SSI I/O providing flexible connection between cards and allowing a single SSI master to output the signal to other slave modules. SSI signals are designed for card synchronization only, not external devices. In the PXI Express form factor, the PXI trigger bus built on the PXI Express backplane provides the necessary timing signal connections. All SSI signals are routed to the XJ4 connector, with no requirement for additional cabling. The eight interconnected lines on the PXI Express backplane, labeled PXI Trigger Bus[0:7] provide a flexible interface for syncing multiple modules. The PXIe-9529 utilizes the PXI Trigger Bus [0:7] as a System Synchronization Interface (SSI). Flexible routing of timebase clock and trigger signals onto the PXI Trigger Bus enables the PXIe-9529 to simplify synchronization between multiple modules.The bidirectional SSI I/O provides flexible connection between modules,

allowing the single SSI master PXIe-9529 to output the SSI signals to other slave modules. SSI timing signals and functions are as shown, as is the SSI architecture.

SSI Timing Signal	Functionality
SSI_TIMEBASE	SSI master: issues TIMEBASE SSI slave: accepts SSI_TIMEBASE to replace the internal TIMEBASE signal.
SSI_SYNC_START	SSI master: issues internal SYNC_START SSI slave: accepts SSI_SYNC_START as the digital trigger signal.
SSI_AD_TRIG	SSI master: issues internal AD_TRIG SSI slave: accepts SSI_AD_TRIG as the digital trigger signal.

Table 3-7: SSI Timing Signal Definitions

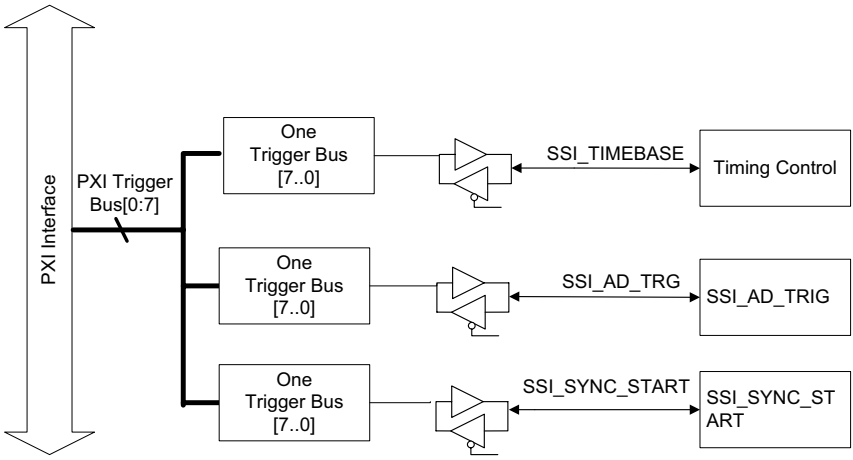


Figure 3-10: SSI Architecture

NOTE:

Different signals cannot be routed onto the same trigger bus line.

The three internal timing signals can be routed to the PXI trigger bus through software drivers. Physically, signal routing is accomplished in the FPGA, with cards connected together through the PXI trigger bus achieving synchronization on the three timing signals, as follows.

3.6.1 SSI_TIMEBASE

As output, the SSI_TIMEBASE signal transmits the onboard ADC timebase through the PXI trigger bus. As input, the PXIe-9529 accepts the SSI_TIMEBASE signal as the source of the timebase.

3.6.2 SSI_SYNC_START

Before a SSI master issues SSI_TRIG to other SSI slaves, SSI_SYNC_START is first asserted by the master card, synchronizing all on-chip ADCs in both SSI Master and SSI Slave modules.

3.6.3 SSI_TRIG

As output, the SSI_TRIG signal reflects the trigger event signal in an acquisition sequence. As input, the PXIe-9529 accepts the SSI_TRIG signal as the trigger event source. The signal is configured in the rising edge-detection mode, with minimum pulse width 8ns.

Appendix A Calibration

This chapter introduces the calibration process to minimize analog input measurement errors.

A.1 Calibration Constant

The PXIe-9529 is factory calibrated before shipment, with associated calibration constants written to the onboard EEPROM. At system boot, the PXIe-9529 driver loads these calibration constants, such that analog input path errors are minimized. ADLINK provides a software API for calibrating the PXIe-9529.

The onboard EEPROM provides two banks for calibration constant storage. Bank 0, the default bank, records the factory calibrated constants, providing written protection preventing erroneous auto-calibration. Bank 1 is user-defined space, provided for storage of self-calibration constants. Upon execution of auto-calibration, the calibration constants are recorded to Bank 1.

When PXIe-9529 boots, the driver accesses the calibration constants and is automatically set to hardware. In the absence of user assignment, the driver loads constants stored in bank 0. If constants from Bank 1 are to be loaded, the preferred bank can be designated as boot bank by software. Following re-assignment of the bank, the driver will load the desired constants on system reboot. This setting is recorded to EEPROM and is retained until reconfiguration.

A.2 Auto-Calibration

Because errors in measurement and outputs will vary with time and temperature, re-calibration is recommended when the module is installed. Auto-calibration can measure and minimize errors without external signal connections, reference voltages, or measurement devices.

The PXIe-9529 has an on-board calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured on the production line and recorded in the on-board EEPROM.

Before initializing auto-calibration, it is recommended to warm up the PXIe-9529 for at least 20 minutes and remove connected cables.

NOTE:

It is not necessary to manually factor delay into applications, as the PXIe-9529 driver automatically adds the compensation time.

Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced with an incorrect type; please dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Contact us should you require any service or assistance.

ADLINK Technology, Inc.
Address: 9F, No.166 Jian Yi Road, Zhonghe District
New Taipei City 235, Taiwan
新北市中和區建一路 166 號 9 樓
Tel: +886-2-8226-5877
Fax: +886-2-8226-5717
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-360-0222
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203)
300 Fang Chun Rd., Zhangjiang Hi-Tech Park,
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1,
Shang Di East Rd., Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8626
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7,
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11, D-68163, Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

ADLINK Technology, Inc. (French Liaison Office)
Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4
神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 서울시 서초구 서초동 1675-12 모인터빌딩 8 층
8F Mointer B/D,1675-12, Seocho-Dong, Seocho-Gu,
Seoul 137-070, Korea
Tel: +82-2-2057-0565
Fax: +82-2-2057-0563
Email: korea@adlinktech.com

ADLINK Technology Singapore Pte. Ltd.
Address: 84 Genting Lane #07-02A, Cityneon Design Centre,
Singapore 349584
Tel: +65-6844-2261
Fax: +65-6844-2263
Email: singapore@adlinktech.com

ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)
Address: 1st Floor, #50-56 (Between 16th/17th Cross) Margosa Plaza,
Margosa Main Road, Malleswaram, Bangalore-560055, India
Tel: +91-80-65605817, +91-80-42246107
Fax: +91-80-23464606
Email: india@adlinktech.com

ADLINK Technology, Inc. (Israeli Liaison Office)
Address: 6 Hasadna St., Kfar Saba 44424, Israel
Tel: +972-9-7446541
Fax: +972-9-7446542
Email: israel@adlinktech.com