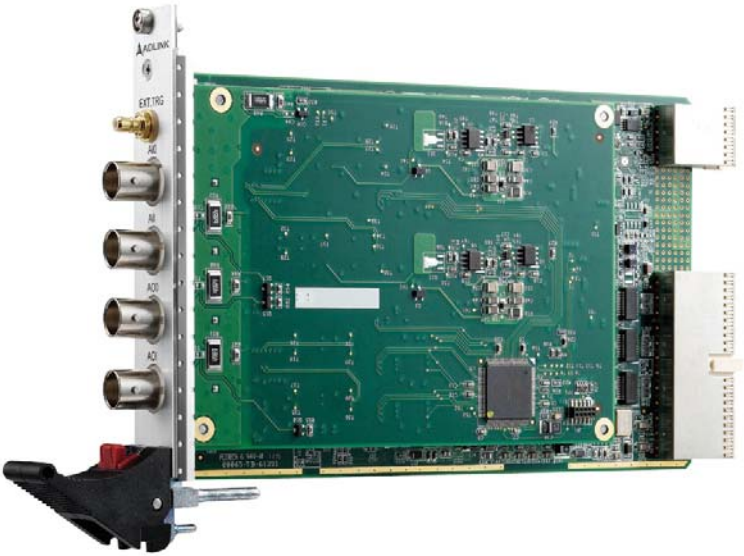
# PXI-9527

24-Bit High Resolution Dynamic
Signal Acquisition and Generation Module

**User's Manual**

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# Revision History

| Revision | Release Date | Description of Change(s) |
|---|---|---|
| 2.00 | 2011/11/17 | Initial Release |

# Preface

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## Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.


Additional information, aids, and tips that help users perform tasks.


Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.


Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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# 1 Introduction

The PXI-9527 is a high-performance 2-CH analog input and output dynamic signal acquisition module, specifically suited for use in audio testing, acoustic measurement, and vibration analysis applications.

The PXI-9527 features two 24-bit simultaneous sampling analog input channels. A 24-bit sigma-delta ADC provides a sampling rate up to 432 kS/s at high resolutions, suitable for higher bandwidth dynamic signal measurements. The sampling rate can be adjusted by setting the onboard DDS clock source to an appropriate frequency. All channels are sampled simultaneously and accept an input range from ±40 V to ±0.316 V. The PXI-9527 analog input supports software selectable AC or DC coupling and 4 mA bias current for integrated electronic piezoelectric (IEPE) sensors.

The PXI-9527 also provides two channels of 24-bit resolution, high fidelity analog output. The outputs occur simultaneously at software programmable rates up to 216 kS/s. A software programmable output range of 0.1 V, 1 V, and 10 V is available on the output channels.

## 1.1 Features

- PXI specification Rev. 2.2 compliant
- 24-Bit Sigma-Delta ADC and DAC
- 2-CH simultaneous sampling analog inputs
- 2-CH simultaneous updated analog outputs
- 432 kS/s maximum ADC sampling rate with software programmable rate
- 216 kS/s maximum DAC update rate with software programmable rate
- Programmable input range: ±40 V, ±10 V, ±3.16 V, ±1 V, ±0.316 V
- Programmable output range: ±0.1 V, ±1 V, ±10 V
- AC or DC input coupling, software selectable
- Trigger I/O connector for external digital trigger signal
- Support for IEPE output on each analog input, software-configurable

## 1.2 Applications

- Audio signal testing
- Acoustic measurement
- Environmental noise testing
- Vibration testing
- Machine condition monitoring

## 1.3 Specifications

### 1.3.1 Analog Input

| Channel Characteristics | |
|---|---|
| Channels | 2 |
| Input configurations | Differential or pseudo-differential |
| Input coupling | AC or DC, software selectable |
| ADC resolution | 24 bit |
| ADC type | Delta-sigma |
| Sample rates (fs) | 432 kS/s maximum, 2 kS/s to 432 kS/s in 454.7 uS/s increments, maximum |
| FIFO buffer size | Total 4096 samples shared for AI channels |
| Data transfers | Direct memory access (DMA) |
| Input signal range | ±40 V<br>±10 V<br>±3.16 V<br>±1 V<br>±0.316 V |
| Input Common Mode Range | ±10 V for both differential and pseudo-differential configuration |
| Overvoltage protection | Differential input: ±40 Vpk<br>Pseudo-differential<br>▶ Positive terminal: ±40 Vpk<br>▶ Negative terminal: ±10 Vpk |
| Input impedance | Differential configuration<br>▶ Between (+) and GND: 1 MΩ<br>▶ Between (-) and GND: 1 MΩ<br>Pseudo-differential configuration<br>▶ Between (+) and GND: 1 MΩ<br>▶ Between (-) and GND: 50 Ω |

**Table 1-1: Channel Characteristics**

| Crosstalk | |
|---|---|
| | **Crosstalk** |
| Adjacent channel | < -100 dB |
| *Measured with +/-10V input*<br>*Input signal is 18 Vpp @ 1kHz sine wave* | |

**Table 1-2: Crosstalk**

| Transfer Characteristics | | |
|---|---|---|
| | **Input range** | **Offset (±mV) @ Tcal ± 5°C** |
| **AI offset error** | ±40 V | 0.5 |
| | ±10 V | 0.2 |
| | ±3.16 V | 0.1 |
| | ±1 V | 0.05 |
| | ±0.316 V | 0.05 |
| **AI gain error** | ±10 V, ±3.16 V, ±1 V, ±0.316 V | ±0.2% |
| | ±40 V | ±0.5% |

**Table 1-3: Transfer Characteristics**

| Analog Input Channel Bandwidth | |
|---|---|
| **Input range** | **Bandwidth (-3dB)** |
| ±40 V, ±10 V, ±3.16 V, ±1 V, and ±0.316 V | 130 kHz |

**Table 1-4: Analog Input Channel Bandwidth**

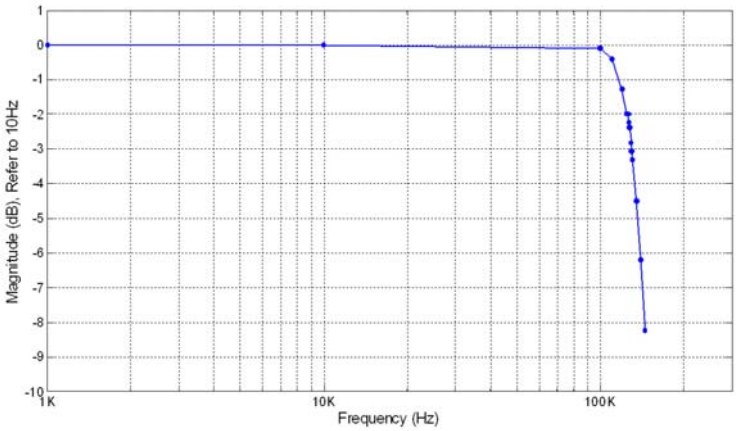



**Figure 1-1: Analog Input Channel Bandwidth, ±10 V Input Range**

| AC Coupling | |
|---|---|
| -3 dB cutoff frequency | 3.5 Hz |
| -0.1 dB cutoff frequency | 26 Hz |

**Table 1-5: AC Coupling**

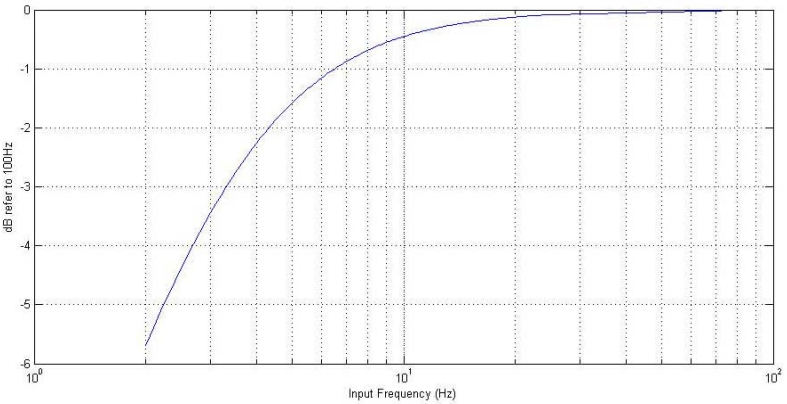



**Figure 1-2: Magnitude Response of AC Couple of Input Channel**

| Integrated Electronic Piezoelectric (IEPE) | |
|---|---|
| Current | 4 mA, each channel independently software selectable |
| Compliance | 24 V |

**Table 1-6: Integrated Electronic Piezoelectric (IEPE)**

### 1.3.2 Analog Output

| Channel Characteristics | |
|---|---|
| Channels | 2 |
| Output configurations | Differential or pseudo-differential (50 Ω to chassis ground), balance output, each channel independently software selectable |
| Output coupling | DC |
| DAC resolution | 24 bit |
| DAC type | Delta-sigma |
| Update rates (fs) | 1 kS/s to 216 kS/s in 227.3 uS/s increments, maximum |
| Minimum working load | 600 Ω |
| Short circuit protection | Indefinite protection between positive and negative |
| Onboard FIFO buffer size | 2048 samples for each AO channel |
| Data transfers | Direct memory access (DMA) |
| Output signal range | ±10 V<br>±1 V<br>±0.1 V |

**Table 1-7: Channel Characteristics**

| AO DC Accuracy | | |
|---|---|---|
| | Output Range | |
| AO Offset ±mV | ±10 V | 1 |
| | ±1 V | 0.25 |
| | ±0.1 V | 0.05 |
| AO Gain Error ±% | ±10 V | 0.4 |
| | ±1 V | 0.4 |
| | ±0.1 V | 0.4 |

**Table 1-8: AO DC Accuracy**

| Output Impedance | | |
|---|---|---|
| | **Differential configuration** | **Pseudo-differential configuration** |
| Between positive output and chassis ground | 50 KΩ | 10 KΩ |
| Between negative output and chassis ground | 50 KΩ | 50 Ω |
| Between positive and negative outputs | 10 KΩ | 10 KΩ |

**Table 1-9: Output Impedance**

| AO Dynamic Characteristics | |
|---|---|
| Bandwidth (-3dB) | 110 kHz |
| AO THD + N | 100 Hz - 20 kHz, 200 kS/s |
| ±0.1V | -89 dB |
| ±1 V | -101 dB |
| ±10V | -101 dB |

**Table 1-10: AO Dynamic Characteristics**

### 1.3.3 Triggers, Timebase

| Triggers | |
|---|---|
| Trigger source | Software command, analog input, external digital trigger, PXI star trigger, and PXI trigger bus [0..7] |
| Trigger mode | Post trigger, delay trigger |

**Table 1-11: Triggers**

| Analog Trigger | |
|---|---|
| Source | AI0 - AI1 |
| Level | ± Full-scale, programmable |
| Trigger conditions | Positive or negative |
| Trigger resolution | 24 bit |

**Table 1-12: Analog Trigger**

| Digital Trigger | |
|---|---|
| Sources | Front panel SMB connector |
| Compatibility | 5V TTL |
| Trigger polarity | Rising or falling edge |
| Pulse width | 65 ns minimum |

**Table 1-13: Digital Trigger**

| Timebase | |
|---|---|
| Frequency | 80 MHz |
| Internal Timebase Accuracy | ±20 ppm, over operating temperature range |

**Table 1-14: Timebase**

### 1.3.4 General Specifications

| Bus and Physical | |
|---|---|
| Bus interface | PCI, 32 bit/ 33MHz |
| PCI Bus Signaling | Universal PCI, support 3.3 V and 5 V PCI signals |
| Physical dimensions | 160 W x 100 H mm (6.3 x 3.94 in.) |

| Environment Requirements | |
|---|---|
| Operating environment | Temperature:0°C - 50°C<br>Relative humidity: 5% - 95%, non-condensing |
| Storage Environment | Temperature: -20°C - +80°C<br>Relative humidity: 5% - 95%, non-condensing |

| Calibration | |
|---|---|
| Onboard reference | +5 V |
| Temperature coefficient | ≤ ±5 ppm/°C |
| Self-calibration | On software command, the PXI-9527 corrects offset and gain error relative to internal high stability, high precision reference |
| External calibration interval | 1 year |
| Warm-up time | 15 minutes |

| Power Consumption | | |
|---|---|---|
| **Power Rail** | **Standby Current (mA)** | **Full Load (mA)** |
| +5 V | 930 | 2330 |
| +12 V | 310 | 350 |

## 1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW®.

All software options are included in the ADLINK All-in-One CD. Commercial software drivers are protected with licensing codes. Without the code, you may install and run the demo version for trial/demonstration purposes for only up to two hours. Contact your ADLINK dealer to purchase the software license.

### 1.4.1 SDK

For customers who want to write their own programs, ADLINK provides the following software development kits.

- ▷ DAQPilot for Windows, compatible with various application environments, such as VB.NET, VC.NET, VB/VC++, BCB, and Delphi
- ▷ DAQPilot for LabVIEW
- ▷ Toolbox adapter for MATLAB

### 1.4.2 DSA-DASK

DSA-DASK includes device drivers and DLL for Windows 2000/XP/Vista/7. DLL is binary compatible across Windows 2000/XP/Vista/7. This means all applications developed with DSA-DASK are compatible with these Windows operating systems. The development environment may be VB.NET, VC.NET, VB/VC++, BCB, and Delphi, or any Windows programming language that allows calls to a DLL. The DSA-DASK user and function reference manuals are on the ADLINK All-in-One CD.

### 1.4.3 Application Software

ADLINK's Dynamic Signal Assistant is a ready-to-run software utility designed for dynamic signal acquisition modules, such as the PXI-9527. This software provides a windows-based configuration interface for setting parameters, in addition to a real-time visualized data display on the screen. An instrument-like user interface is also provided for basic waveform generation. The Dynamic Signal Assistant can also log data acquired from hardware modules. With the Dynamic Signal Assistant, signal acquisition and generation can be performed in just a few minutes with no programming required. A brief overview of the application's operations follows.

The Device Setting window allows selection of a virtual device or any installed ADLINK DSA devices. Selecting an Operation Mode allows separate or simultaneous AI and AO operation.

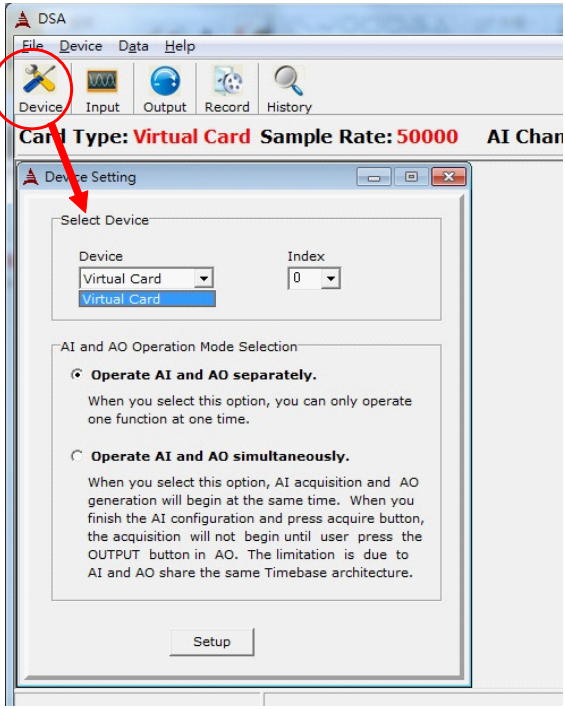



**Figure 1-3: DSA Device Setting Interface**

The Input window provides operation of AI channels, such as:

- Channel configuration: change AI channels settings and start/stop acquisition
- Time domain chart: displays acquired data with time domain mode
- Freq domain chart: calculates acquired data frequency response and displays the result
- Zoom, copy, save, and print operations for chart images are all provided by buttons above the displayed charts

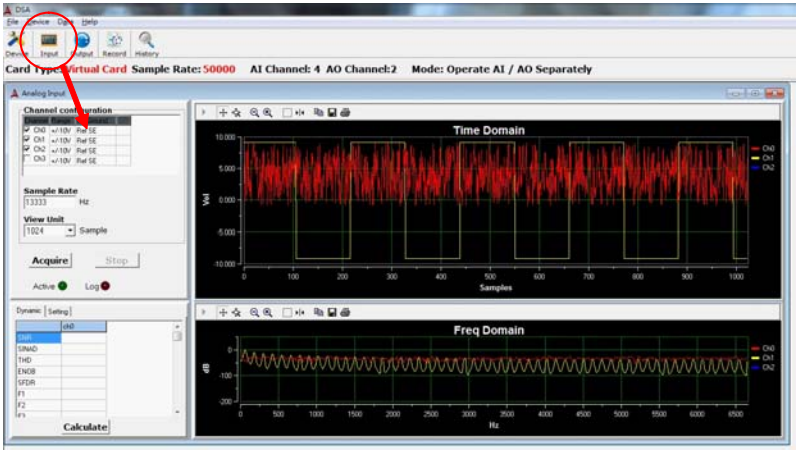



**Figure 1-4: DSA Input Interface**

The Output window provides operation of AI channels, such as:

- Output of offset, amplitude, frequency, and phase can be set by, first, settings at the left
- Input of the desired number is enabled via the center key-pad
- Channels can be enabled/disabled and preferred output patterns chosen by the bottom buttons
- The top “OUTPUT” button executes AO channel output

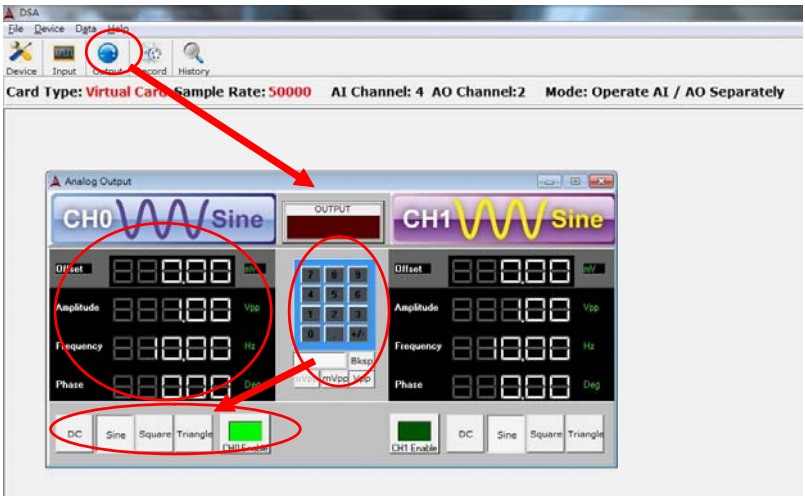



**Figure 1-5: DSA Output Interface**

# 2 Getting Started

This chapter describes proper installation environment, installation procedures, package contents and basic information users should be aware of regarding the PXI-9527.


NOTE:

Diagrams and illustrated equipment are for reference only. Actual system configuration and specifications may vary.

## 2.1 Installation Environment

When unpacking and preparing to install, please refer to Important Safety Instructions.

Only install equipment in well-lit areas on flat, sturdy surfaces with access to basic tools such as flat- and cross-head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools

- Phillips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Antistatic mat

ADLINK PXI-9527 DAQ modules are electrostatically sensitive and can be easily damaged by static electricity. The module must be handled on a grounded anti-static mat. The operator must wear an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the carton and packaging for damage. Shipping and handling could cause damage to the equipment inside. Make sure that the equipment and its associated components have no damage before installation.


The equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing.

## 2.2 Package Contents

Before continuing, check the package contents for any damage and ensure that the following items are included:

- PXI-9527 dynamic signal acquisition and generation module
- ADLINK All-in-one compact disc
- PXI-9527 User's Manual

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.


Do not install or apply power to equipment that is damaged or missing components. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/vendor immediately for assistance and obtain authorization before returning any product.

## 2.3 Device Layout and IO Array

NOTE:

All dimensions are in mm

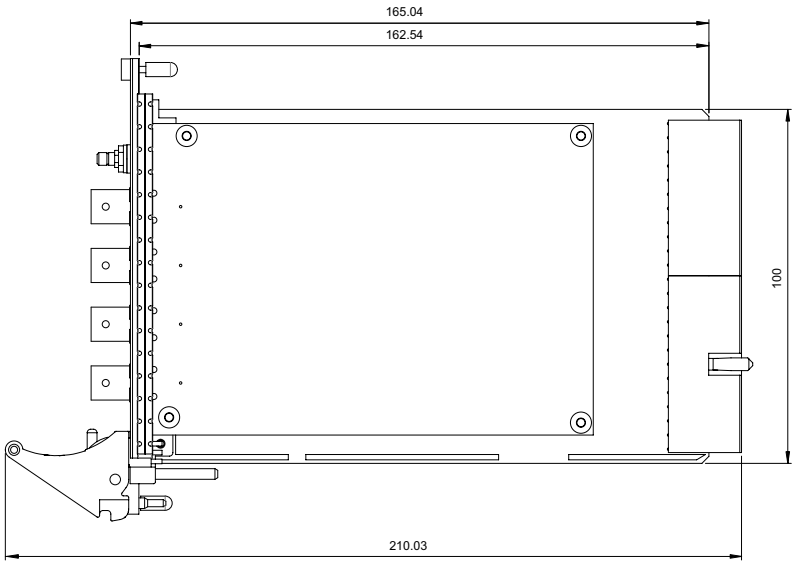



**Figure 2-1: PXI-9527 Side View**

The PXI-9527 I/O array is labeled to indicate connectivity, as shown.

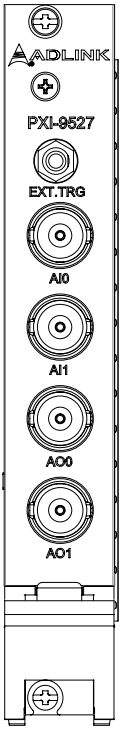



**Figure 2-2: PXI-9527 I/O array**

## 2.4 Installing the module

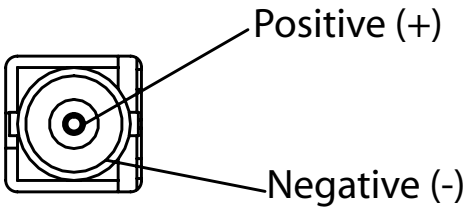
1. Turn off the PXI system/chassis and disconnect the power cable from the power source.
2. Align the module's edge with the module guide in the PXI chassis.
3. Slide the module into the chassis until resistance is felt from the PXI connector.
4. Push the ejector upwards and fully insert the module into the chassis.

5. Once the module is fully seated, a “click” can be heard from the ejector latch.
6. Tighten the screw on the front panel.
7. Connect the power plug to a power source and turn on the PXI system/chassis.

## 2.5 Signal Connection

### 2.5.1 BNC Connector Polarity

BNC connector polarity is as shown.




### 2.5.2 Analog Input Connection

The PXI-9527 input channels can be configured as differential for ground-reference signal sources, and for floating signal sources, as pseudo-differential, to provide a reference. In pseudo-differential configuration, the (-) port is grounded through a 50 Ω resistor.

| Signal Source Type | AI Channel Configuration |
|---|---|
| Floating | Pseudo differential |
| Ground-Reference | Differential |

**Table 2-1: Analog Input Connection**

### 2.5.3 Analog Output Connection

If the DUT inputs are ground-referenced, differential output mode can eliminate measurement errors caused by ground loops.

If the DUT inputs are in a floating system, such as a floating earphone, pseudo-differential output mode provides a reference ground connected to the positive output of the BNC through a 50 Ω resistor.

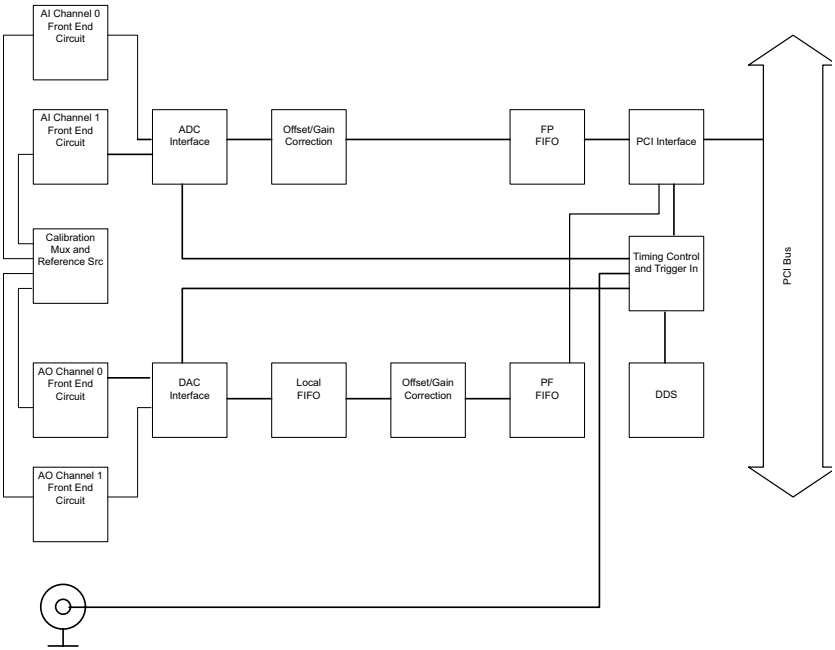
| DUT Input Reference Type | AO Channel Configuration |
|---|---|
| Floating | Pseudo differential |
| Ground-Reference | Differential |

**Table 2-2: Analog Output Connection**

# 3 Operations

This chapter contains information regarding analog input, analog output, triggering and timing for the PXI-9527.

## 3.1 Functional Block Diagram



## 3.2 Analog Input Channel

### 3.2.1 Analog Input Front-End Configuration

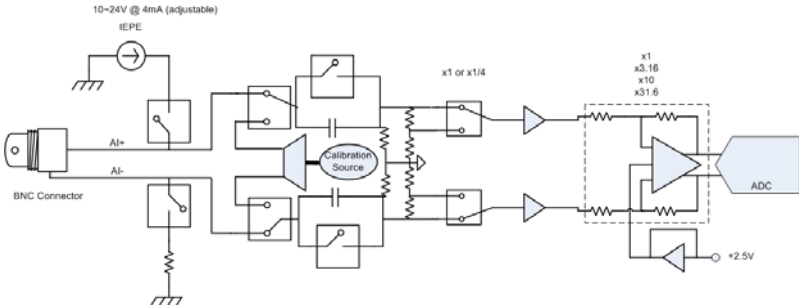



**Figure 3-1: Analog Input Architecture of the PXI-9527**

#### Differential and Pseudo-Differential Input Configuration

The PXC-9527 provides both differential and psuedo-differential input configurations. The differential input mode provides voltage to the anode and cathode inputs of the BNC connector according to signal voltage difference between them. If the signal source is ground-referenced, the differential input mode can be used for common-mode noise rejection.

If the signal source is a floating signal, pseudo-differential input mode will provide a reference ground connected to the cathode input of the BNC through a 50 Ω resistor. This will prevent the floating source from drifting over the input common-mode range.

The recommended configurations for the signal sources are as follows..

| Signal Source Type | Card Configuration |
|---|---|
| Floating | Pseudo differential |
| Ground-Reference | Differential |

**Table 3-1: Input Configurations**

**AC and DC Input Coupling**

AC and DC coupling are available. With DC coupling, DC offset present in the input signal is passed to ADC. DC coupling is indicated if the signal source has a small level of offset voltage or if DC content of the signal is important.

In AC coupling, the DC offset present in the input signal is erased. AC coupling is indicated if the DC content of the input signals is to be rejected. AC coupling enables a high pass R-C filter through the input signal path. The corner frequency (-3dB) is about 3Hz.

**Input for IEPE**

For applications that require sensors such as accelerometers or microphones, PXI-9527 provides an excitation current source.

The common excitation current is usually about 4mA for these IEPE sensors. A DC voltage offset is generated due to the excitation current and sensor impedance. When IEPE current sources are enabled, the PXI-9527 automatically sets input configuration to AC coupling.

### 3.2.2 Input Range and Data Format

When using an A/D converter, properties of the signal to be measured should be considered prior to selecting channel and signal connection to the module. Please refer to Section 2.5: Signal Connection.

A/D acquisition is initiated by a trigger source, which must be predetermined. Data acquisition will commence once the trigger condition is established. Following completion of A/D conversion, A/D data is buffered in a Data FIFO, and can then be transferred to PC memory for further processing.

Transfer characteristics of various input ranges of the PXI-9527 are as follows. Data format of the PXI-9527 is 2's complement.

| Description | Full-scale range | Least significant bit | FSR-1LSB | -FSR |
|---|---|---|---|---|
| Bipolar Analog Input | ±40 V | 4.76 uV | 39.99999952 V | -40 V |
| | ±10 V | 1.19 uV | 9.99999881 V | -10 V |
| | ±3.1622776V | 0.37uV | 3.1622773 V | -3.1622776 V |
| | ±1V | 0.119 uV | 0.999999881V | -1 V |
| | ±0.316227 V | 0.037uV | 0.31622773 V | -0.31622776 V |
| Digital Code | N/A | N/A | 7FFFFF | 800000 |

**Table 3-2: Input Range and Data Format**

| Description | Midscale +1LSB | Midscale | Midscale –1LSB |
|---|---|---|---|
| Bipolar Analog Input | 4.76 uV | 0 V | -4.76 uV |
| | 1.19 V | 0 V | -1.19 V |
| | 0.37uV | 0 V | -0.37uV |
| | 0.119 uV | 0 V | -0.119 uV |
| | 0.037 uV | 0 V | -0.037 uV |
| Digital Code | 000001 | 000000 | -FFFFFF |

**Table 3-3: Input Range Midscale Values**

### 3.2.3 ADC and Analog Input Filter

**ADC (Analog-to-Digital Converter)**

The PXI-9527 provides sigma-delta analog-to-digital converters, suitable for vibration, audio, and acoustic measurement. The analog side of the sigma-delta ADC is 1-bit, and the digital side performs oversampling, noise shaping and digital filtering. For example, if a desired sampling rate is 108kS/s, each ADC samples input signals at 6.912MS/s, 64 times the sampling rate. The 1-bit 6.912MS/s data streams from 1-bit ADC to its internal digital filter circuit to produce 24-bit data at 108kS/s. The noise shaping removes quantization noise from low frequency to high frequency. With the digital filter at the last stage, the digital filter improves the ADC resolution and removes high frequency quantization noise.

The relationship between ADC sample rate and DDS output clock is as follows

| Sampling Rate | 2 K - 54 kHz | 54 K - 108 kHz | 108 K-216 kHz | 216 K - 432 kHz |
|---|---|---|---|---|
| DDS CLK | 512 K - 13.824 MHz | 6.912 M- 13.824 MHz | 6.912 M- 13.824 MHz | 13.824 M - 27.648 MHz |

**Table 3-4: ADC Sample Rates VS DSS Output Clock**

**Filter**

Each channel has a two-pole low pass filter. The filters limit the bandwidth of the signal path and reject band noise.

### 3.2.4 FIFO and DMA Transfer For Analog Input

**FIFO**

One FIFO is implemented on the PXI-9527 for analog input data storage. FIFO depth is 4096 samples, shared between both AI channels. When only one AI channel is enabled, the 4096-sample-FIFO is used for one-channel data storage. When both are enabled, the 4096-sample-FIFO is shared between both channels.

### Bus-Mastering Dma Data Transfer

PCI bus-mastering DMA is essential for continuous data streaming, as it helps to achieve full potential PCI bus bandwidth and improve bus efficiency. The bus-mastering controller controls the PCI bus, with the host CPU unburdened, since data is directly transferred to the host memory without intervention. Once analog input begins, the DMA returns control of the program. During DMA transfer, the hardware temporarily stores acquired data in the onboard AD Data FIFO, and then transfers the data to a user-defined DMA buffer in the computer.

Using a high-level programming library for high speed DMA data acquisition, the sampling period and number of conversions need only be assigned to their specified counters. After the AD trigger condition is met, data is transferred to the system memory by the bus-mastering DMA.

In a multi-user or multi-tasking OS, such as Microsoft Windows, Linux, or other, it can be difficult to allocate a large continuous memory block. Therefore, the PCI controller provides DMA transfer with scatter-gather function to link non-continuous memory blocks into a linked list allowing transfer of large amounts of data without being limited by memory limitations. In non-scatter-gather mode, the maximum DMA data transfer size is 2 MB double words (8 MB bytes); in scatter-gather mode, there is no limitation on DMA data transfer size beyond physical storage capacity of the system. Users can also link descriptor nodes circularly to achieve a multi-buffered DMA. As shown, in a linked list comprising three DMA descriptors, each containing a PCI address, PCI dual address, transfer size, and the pointer to the next descriptor, PCI address and PCI dual address support 64-bit addresses which can be mapped into more than 4 GB of address space.

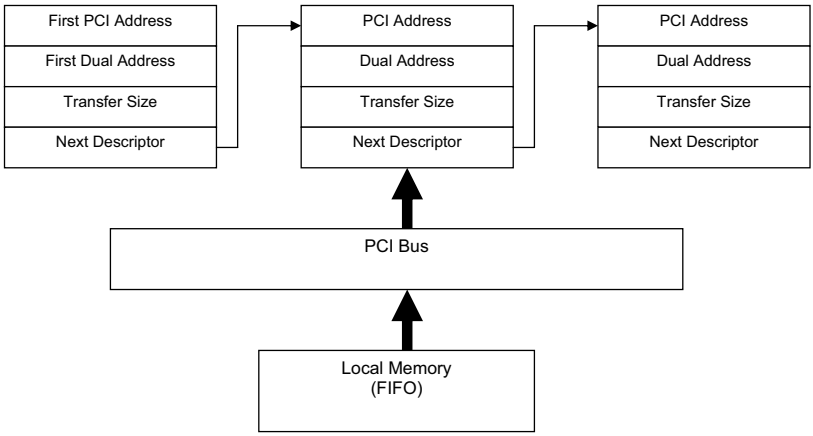



**Figure 3-2: Linked List of PCI Address DMA Descriptors**

## 3.3 Analog Output Channel

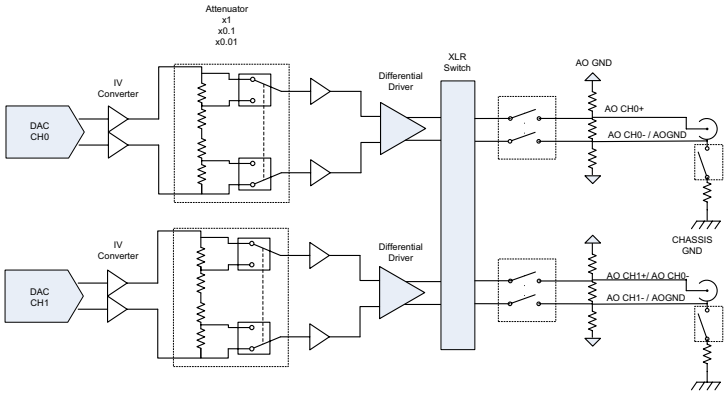



**Figure 3-3: Analog Output Architecture of the PXI-9527**

### 3.3.1 Analog Output Front-End Configuration

#### Differential and Pseudo-Differential Output Configuration

Differential output provides voltage to the anode and cathode outputs of the BNC connector according to DAC output voltage difference between the two. If the DUT inputs are ground-referenced, the differential output mode can be used for the elimination of measurement errors caused by ground loops.

If the DUT inputs are in a floating system, such as a floating earphone, pseudo-differential output mode provides a reference ground connected to the cathode output of the BNC through a 50 Ω resistor. This prevents the floating system from drifting beyond its input common-mode range.

The recommended configurations for DUT input reference types are as follows.

| DUT Input Reference Type | Card Configuration |
|---|---|
| Floating | Pseudo-differential |
| Ground-reference | Differential |

**Table 3-5: Output Configuration**

### 3.3.2 Output Range and Data Format

Ideal PXI-9527 transfer characteristics for various input codes versus output voltages are as follows. The PXI-9527 data format is 2's-complement.

| Description | Digital Input Code | Bipolar Analog Output | | |
|---|---|---|---|---|
| Full-scale range | N/A | ±10 V | ±1 V | ±0.1 V |
| Least significant bit | N/A | 1.19uV | 0.119uV | 0.012uV |
| FSR-1LSB | 7FFFFF | 9.99999881 V | 0.999999881 V | 0.099999988 V |
| Midscale +1LSB | 000001 | 1.19 uV | 0.119 uV | 0.012 uV |
| Midscale | 000000 | 0 V | 0 V | 0 V |

**Table 3-6: Digital Input Code and Analog Output Range**

| Description | Digital Input Code | Bipolar Analog Output | | |
|---|---|---|---|---|
| Midscale –1LSB | FFFFFF | -1.19 uV | -0.119 uV | -0.012 uV |
| -FSR | 800000 | -10 V | -1 V | -0.1 V |

**Table 3-6: Digital Input Code and Analog Output Range**

### 3.3.3 DAC and Analog Output Filter

#### DAC (Digital-to-Analog Converter)

The PXI-9527 provides two 24-bit delta-sigma DACs, separating sample rates into four regions between 1kS/s and 216kS/s, as shown in Table 3-7, “DAC (Digital-to-Analog Converter)”. Different bandwidths of internal digital filter for each region optimize DA dynamic performance over all sample rate regions. For example, lower sample rates correspond to a lowered digital filter bandwidth. SNR of the output current is improved and the requirement for external analog low pass filtering is eliminated.

The relationship between DAC sample rate and DDS output clock is as follows

| Update Rate | 1K-27kHz | 27K-54kHz | 54K-108kHz | 108K-216kHz |
|---|---|---|---|---|
| DDS CLK | 512 K-13.824 MHz | 6.912 M-13.824 MHz | 6.912 M-13.824 MHz | 13.824 M-27.648 MHz |

**Table 3-7: DAC (Digital-to-Analog Converter)**

#### Analog Front-End Filter

Each channel has a 3-pole low pass filter. The cutoff frequency is set at 110 kHz to limit the bandwidth of the signal path and eliminate most out-of-band images and noise.

### 3.3.4 FIFO and DMA Transfer For Analog Output

#### FIFO

The PXI-9527 implements two FIFOs for analog output, each having a depth of 2048 samples.

**Bus-mastering DMA Data Transfer**

For analog output, data is transferred from host PC memory to onboard FIFO by DMA transfer. Please see Section 3.2.4: FIFO and DMA Transfer For Analog Input for a detailed description.

## 3.4 Trigger Source and Trigger Mode

This section details PXI-9527 triggering operations. Since AI and AO share the same trigger source, when their operations are simultaneously enabled, the trigger signal is valid only when both are ready to receive the trigger signal. For more details of programming the PXI-9527, please refer to the software operation manual.

### 3.4.1 Trigger Sources

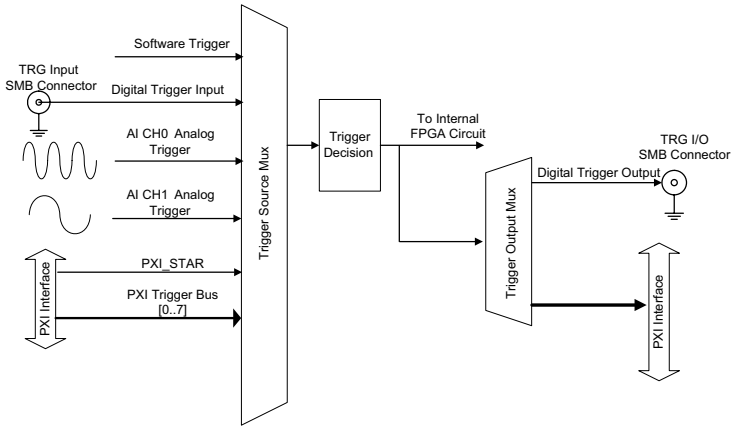



**Figure 3-4: Trigger Architecture of the PXI-9527**

The PXI-9527 requires a trigger to implement acquisition of data. Configuration of triggers requires identification of trigger source. The PXI-9527 supports internal software trigger, external digital trigger, PXI_STAR trigger, PXI Trigger Bus [0.7], and SSI bus as well as analog trigger.

### Software Trigger

The software trigger, generated by software command, is asserted immediately following execution of specified function calls to begin the operation.

### External Digital Trigger

An external digital trigger is generated when a TTL rising edge or a falling edge is detected at the SMB connector on the front panel. As shown, trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL compatible, and the minimum pulse width is 65 ns.

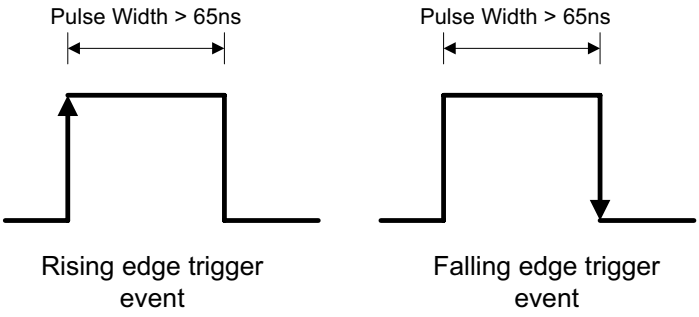



**Figure 3-5: External Digital Trigger**

### PXI STAR Trigger

When PXI STAR is selected as the trigger source, the PXI-9527 accepts a TTL-compatible digital signal as a trigger signal. The trigger occurs when a rising edge or falling edge is detected at PXI STAR, with trigger polarity configurable by software. The minimum pulse width requirement of this digital trigger signal is 65 ns.

### PXI Trigger Bus

The PXI-9527 utilizes PXI Trigger Bus Numbers 0 through 7 to act as a System Synchronization Interface (SSI). With the inter-

connected bus provided by PXI Trigger Bus, multiple modules are easily synched. When configured as input, the PXI-9527 serves as a slave module and can accept trigger signals from one of buses 0 through 7. When configured as output, the PXI-9527 serves as a master module and can output trigger signals to the PXI Trigger Bus Numbers 0 through 7.

### Analog Trigger

The PXI-9527 analog trigger circuitry can be configured to monitor one analog input channel from which data is acquired. Selection of an analog input channel as the analog trigger channel does not influence the input channel acquisition operation. The analog trigger circuit generates an internal digital trigger signal based on the condition between the analog signal and the defined trigger level.

Analog trigger conditions are as follows:

- ▷ Positive-slope trigger: The trigger event occurs when the analog input signal changes from a voltage lower than the specified trigger level to a voltage exceeding the specified trigger level.
- ▷ Negative-slope trigger: The trigger event occurs when the analog input signal changes from a voltage exceeding the specified trigger level to a voltage lower than the specified trigger level.

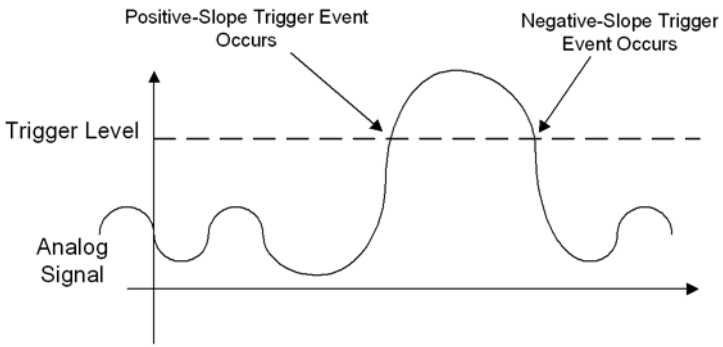



**Figure 3-6: Analog Trigger Conditions**

**Trigger Export**

The PCI/PXI-9527 can export trigger signals to the SMB TRG IO on the front panel, and PXI Trigger Bus Numbers 0 through 7. The TRG IO on the front panel can also be programmed to output the trigger signal when the trigger source is generated by software, PXI STAR, or PXI Trigger Bus Numbers 0 through 7. The PXI-9527 utilizes PXI Trigger Bus Numbers 0 through 7 to act as the System Synchronization Interface. When configured as the output, the PXI-9527 serves as a master module and can output trigger signals to synchronize the slave modules. The trigger signal can be routed to any of the seven PXI Trigger Bus Numbers via software.

### 3.4.2 Trigger Mode

Two trigger modes applied to trigger sources initiate different data acquisition timings when a trigger event occurs. The following trigger mode descriptions are applied to analog input and analog output functions.

**Post Trigger Mode**

If post trigger mode is configured, activity commences once the following trigger conditions are met:

- ▷ The analog input channel acquires a programmed number of samples at a specified sampling rate
- ▷ The analog output channel outputs pre-defined voltage at a specified output rate

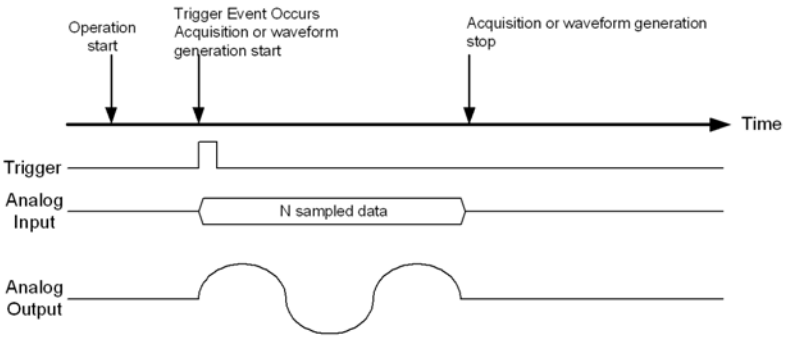


Figure 3-7: Post-trigger Acquisition / Waveform Generation

### Delay Trigger Mode

If delay trigger mode is configured, delay time from when the trigger event asserts to the beginning of the acquisition and waveform generation can be specified, as shown. Delay time is specified by a 32-bit counter value with the counter clocking based on the PCI clock. Accordingly, maximum delay time is the period of PCI_CLK X (232 - 1) and minimum is the period of PCI_CLK.

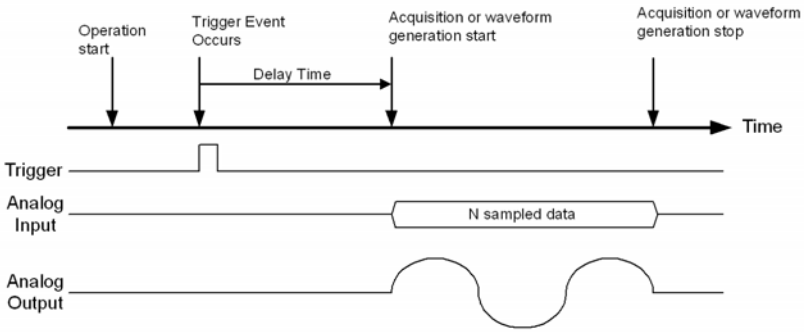



Figure 3-8: Delay Trigger Mode Acquisition / Waveform Generation

## 3.5 ADC and DAC Timing Control

### 3.5.1 Timebase Architecture

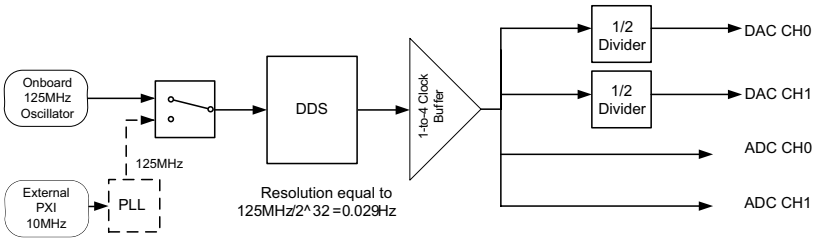



Figure 3-9: PXI-9527 Timebase Architecture

To drive the sigma-delta ADC and DAC, an onboard timebase clock is applied. The timebase clock frequency exceeds the sample rate and is produced by a DDS chip. The output frequency of DDS chip is programmable with excellent resolution. The PXI-9527 accepts the external 10MHz clock from the PXI backplane for better synchronization between modules.

### 3.5.2 DDS Timing VS ADC/DAC Relationship

| Sampling Rate | 2 K - 54 kHz | 54 K - 108 kHz | 108 K - 216 kHz | 216 K - 432 kHz |
|---|---|---|---|---|
| Update Rate | 1K-27 kHz | 27K-54 kHz | 54K-108 kHz | 108K-216 kHz |
| DDS CLK | 512 K-13.824 MHz | 6.912 M-13.824 MHz | 6.912 M-13.824 MHz | 13.824 M-27.648 MHz |

**Table 3-8: Timing Relationship of the ADC, DAC and DDS Clock**

### 3.5.3 Timing Constraints

As described in Section 3.5.1, the ADC and DAC share a single timebase source, that is, the output of the DDS clock. When simultaneous operation of ADC and DAC is implemented, it should be considered that:

- When sampling rate of the ADC is set to before configuring DAC, the update rate of the DAC is limited and fixed correspondingly, and when update rate of the DAC is set before configuring ADC, the sampling rate of DAC is limited and fixed correspondingly, as shown
- Because the ADC and DAC share the same trigger source, both AI and AO operations require coordination prior to trigger event, that is, the trigger event cannot occur before AI & AO configuration is complete

### 3.5.4 Filter Delay in ADC and DAC

The filter delay indicates the time required for data to propagate through a converter. Both AI and AO channels experience filter delay due to the filter circuitry and the architecture of the converter, as shown.

## ADC Filter Delay

| Update Rate (kS/s) | Filter Delay (Samples) |
|---|---|
| 2 K - 54 kS/s | 12 |
| 54 K-108 kS/s | 7 |
| 108 K-216 kS/s | 5 |
| 216 K-432 kS/s | 5 |

**Table 3-9: ADC Filter Delay**

## DAC Filter Delay

| Update Rate (kS/s) | Filter Delay (Samples) |
|---|---|
| 2 K - 54 kS/s | 43.4 |
| 54 K-108 kS/s | 87.5 |
| 108 K-216 kS/s | 176.8 |

**Table 3-10: DAC Filter Delay**

# 4 Calibration

This chapter introduces the calibration process to minimize analog input measurement errors and analog output errors.

## 4.1 Calibration Constant

The PXI-9527 is factory calibrated before shipment, with associated calibration constants written to the onboard EEPROM. At system boot, the PXI-9527 driver loads these calibration constants, such that analog input path and analog output circuit errors are minimized. ADLINK provides a software API for calibrating the PXI-9527.

The onboard EEPROM provides three banks for calibration constant storage. Bank 0, the default bank, records the factory calibrated constants, providing written protection preventing erroneous auto-calibration. Banks 1 and 2, user-defined space, are provided for storage of self-calibration constants. Upon execution of auto-calibration, the calibration constants are recorded to bank 1 or 2 based on user assignment.

When PXI-9527 boots, the driver accesses the calibration constants and is automatically set to hardware. In the absence of user assignment, the driver loads constants stored in bank 0. If constants from bank 1 or 2 are to be loaded, the preferred bank can be designated as boot bank by software. Following re-assignment of the bank, the driver will load the desired constants on system re-boot. This setting is recorded to EEPROM and is retained until re-configuration.

## 4.2 Auto-Calibration

Because errors in measurement and outputs will vary with time and temperature, re-calibration is recommended when the module is installed. Auto-calibration can measure and minimize errors without external signal connections, reference voltages, or measurement devices.

The PXI-9527 has an on-board calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured on the production line and recorded in the on-board EEPROM.

Before initializing auto-calibration, it is recommended to warm up the PXI-9527 for at least 20 minutes and remove connected cables.

## 4.3 Offset Error Compensation During AI Sampling Rate Change

For optimal measurement results, the PXI-9527 is equipped with an internal offset error compensation mechanism to respond to changes in the AI sampling rate. Compensation times required for various sampling rates are shown. For example, when sampling rate is changed from 432 kS/s to 2 kS/s, 6.2 sec is required for offset compensation. When the sampling rate is next set between 2 kS/s and 53.999 kS/s, it is not necessary to have 6.2 sec for the offset compensation. Only a sampling rate set to different ranges will generate a compensation time.


NOTE:

It is not necessary to manually factor delay into applications, as the PXI-9527 driver automatically adds the compensation time.

| Sampling Rate | 2 kS/s - 53.999 kS/s | 54 kS/s - 107.999 kS/s | 108 K/s - 215.999 kS/s | 216 kS/s - 432 kS/s |
|---|---|---|---|---|
| Offset Compensation Time | 6.2 sec | 2.6 sec | 1.3 sec | 0.65 sec |

**Table 4-1: Offset Compensation Time Required for Various Sampling Rates**

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# Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

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Risk of explosion if battery is replaced with an incorrect type; please dispose of used batteries appropriately.

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- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

# Getting Service

Contact us should you require any service or assistance.

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