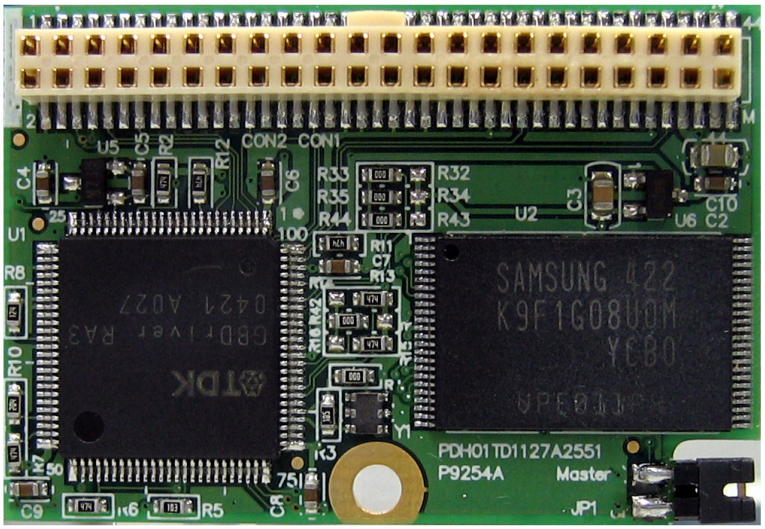
POWER QUOTIENT INTERNATIONAL CO., LTD.

DiskOnModule™

IC STORAGE SPECLALIST

is an IDE storage device using solid-state flash memory technology. It's rugged, reliable and consumes little power. It's an ideal substitute for a hard disk drive, and is a cost-effective solution for applications requiring low power consumption and high mobility for system boot up.



DH Series Datasheet

TAIWAN
POWER QUOTIENT INTERNATIONAL CO., LTD.
Tel: +886-2-82265288
Fax: +886-2-82265268
www.pqi.com.tw

USA
PQI CORPORATION
Tel: +1-510-6517281
Fax: +1-510-6517240
www.pqimemory.com

THE NETHERLANDS
PQI EUROPE B.V.
Tel: +31-73-6273555
Fax: +31-73-6234033
www.pqieurope.com

JAPAN
POWERGLOBAL iNDEX CO., LTD.
Tel: +81-3-58354545
Fax: +81-3-58354540
www.pg-index.com

CHINA - Shenzhen
PQI (Shenzhen) CO., LTD.
Tel: +86-755-83287509
Fax: +86-755-83287582
www.pqi.com.cn

CHINA - Shanghai
PQI (Shanghai) CO., LTD.
Tel: +86-21-64403280
Fax: +86-21-64403279
www.pqi.com.cn

CHINA - Hong Kong
PQI (H.K.) CO., LTD.
Tel: +852-27074118
Fax: +852-27074308
www.pqi.com.cn

Revision History

Revision No	History	Draft Date	Remark
A.0	First document announced.	01/26/05	Preliminary

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Power Quotient International
IC STORAGE SPECIALIST
DiskOnModule™ DH Series

Description

PQI's **DiskOnModule DH series** based on NAND type flash memory controller technology. This product complies with 44 PIN IDE (ATA) standard interface and is suitable for data storage memory medium for portable system. By using **DiskOnModule** it is possible to operate good performance for the portable system which have IDE interface slots.

Features

- High Performance
- Non-volatile Flash Memory
  The DOM is implemented by using NAND type flash memory, which is a high density, non-volatile read/write device. Flash data retention is guaranteed for at least 10 years, with no battery or other power source required.
- 100% True IDE Mode HDD Compatible
- Broad Operating System and Processors Supports
- Capacities 16MB~1.5GB
- Low Power Consumption
- Robust Error Correction
- High Reliability

Introduction

1. About This Manual

This manual provides instructions for the installation and specification of PQI's **DiskOnModule, DiskOnModule** is designed for use in PCs, and their respective compatible computers.

2. What is DiskOnModule?

PQI's **DiskOnModule** is a storage device based on flash memory technology, which emulates an ordinary magnetic hard disk. The **DiskOnModule** series products provide an all in one module solution for solid-state flash disk. The **DiskOnModule** is suitable for use in portable and embedded systems which have limited space and power consumption.

Unlike standard IDE drives, no signal cable and extra, special space is required. The **DiskOnModule** is a solid-state solution for IDE Hard Disk drive, which has no moving parts. That provides a good stability in a moving system.The **DiskOnModule** products are also free from extra and special algorithm or some firmware driver. Just plug the **DiskOnModule** into the IDE slot and play it,users can play the **DiskOnModule** as same as the Hard Disk Drives.

The **DiskOnModule** family provides the capacities ranging from 16MB up to 2GB. In the future, the capacity will be increased up to 4GB.

Specification

Environment Specifications		
Temperature (Industrial)	Operating	0℃ to +70℃
	Non-Operating	-40℃ to +85℃
Temperature (WideTemp)	Operating	-40℃ to +80℃
	Non-Operating	-55℃ to +95℃
Relative Humidity		8% to 95% (with no condensation)
Shock	Operating	1000G
	Non-operating	1000G
Configuration		
Capacity		16Mbytes to 1.5Gbytes
Sector size		512bytes
System Performance		
Media transfer rate *note1	Read	4.3 MB/sec
	Write	3.3 MB/sec
Interface burst transfer rate		
PIO mode 2		8.3 MB/sec
Reliability		
MTBF		1,000,000 hours
ECC		22bit per 256bytes
Power Requirement		
Voltage		DC +3.3V± 5%
		DC +5.0V±10%
Power Consumption		
Read		30mA (typ.)
Write		28mA (typ.)
Stand by		3mA (typ.)

*note1 : There will be different figures shown in different platforms.

Capacity Specifications

Capacity	Cylinder	Head	Sector	Total sectors
16MB	1000	2	16	32000
32MB	500	8	16	64000
64MB	500	8	32	128000
128MB	500	16	32	256000
192MB	750	16	32	384000
256MB	1000	16	32	512000
512MB	1015	16	63	1023120
1024MB	2031	16	63	2047248
1536MB	3047	16	63	3071376

Installation Guide

BEFORE YOU BEGIN

To protect your DOM from static discharge by making sure you are well grounded before touching the DOM. We recommend wearing a grounded wrist strap throughout the installation process.

STEP 1

1. Make sure your computer is turned off before you open the case.
2. Plug the DOM carefully into the IDE slot on your computer or host adapter.
   Caution: Make sure to align pin1 on the computer or host adapter interface connector with pin 1 on your DOM. Pin 1 is indicated by a triangle on the DOM connector.
3. Connect the power cable of the DOM to an unused power connector of the computer.
   Caution: If you need to remove your DOM, use **BOTH HANDS** to carefully pull out it.
4. Check all cable connections and then replace your computer cover.

STEP 2

Before you format or partition your new DOM, you must configure your computer's BIOS so that the computer can recognize your new DOM.

1. Turn your computer on. As your computer start up, watch the screen for a message describing how to run the system setup program (sometimes called BIOS or CMOS setup). This is usually done by pressing a special key, such as DELETE,ESC, or F1, during startup. See your computer manual for details. Press the appropriate key to run the system setup program.
2. If your BIOS provides automatic drive detection (an "AUTO" drive type), select this option. (If you use Normal/CHS mode to partition your DOM, you can get the maximum formatted capacity.)
   This allows your computer to configure itself automatically for your new DOM.
   If your BIOS dose not provide automatic drive detection, select "User-defined" drive setting and enter the CHS values from the table.
   BIOS Settings (see specification)

Capacity (unformatted)	Cylinders	Heads	Sectors

3. Save the settings and exit the System Setup program.
   (your computer will automatically reboot)
   After you configure your computer, you can use the standard DOS commands to partition and format your DOM, as described below.

STEP 3

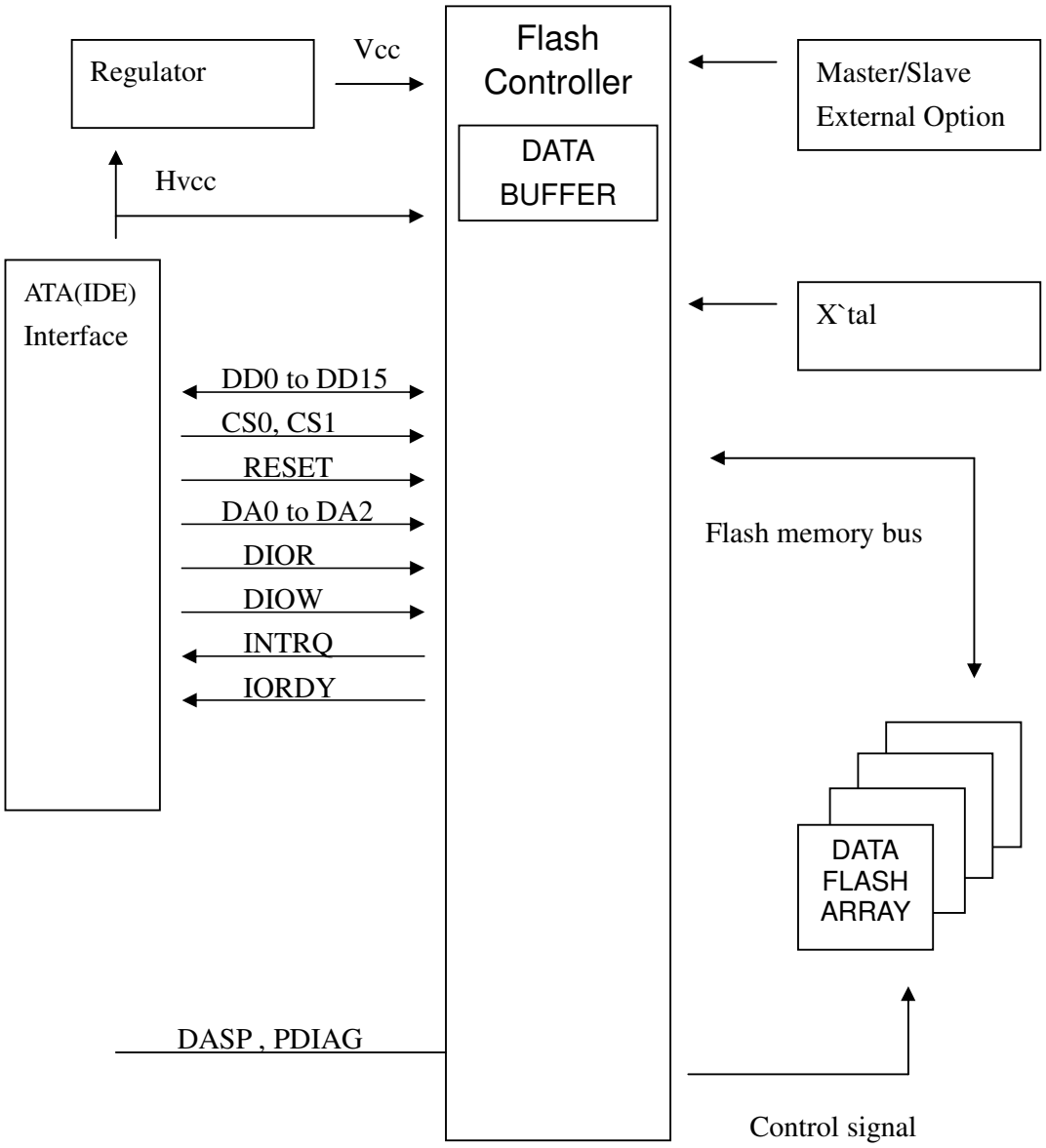
To partition your new DOM, for example use Microsoft® DOS program :

1. Insert a bootable DOS diskette into your diskette drive and restart your computer.
2. Insert a DOS program diskette that contains the **FDISK.EXE** and **FORMAT.COM** programs into your diskette drive. Use the same DOS version that is on your bootable diskette. At the A: prompt, type **FDISK** and press **ENTER**.
3. If you have two **IDE** devices installed, the **FDISK** menu displays five options.

Option five allows you to select the drive you want to partition. Make sure that your new drive is selected.

4. Select "Create DOS partition or logical DOS drive" by pressing 1. Then press ENTER.
5. Select "**Create primary DOS partition**" by pressing **1** again. Then press **ENTER**. Create your first drive partition. If you are creating a partition that will be used to boot your computer (drive C), make sure that the partition is marked active.
6. Create an extended partition and additional logical drives as necessary, until all the space on your new hard drive has been partitioned.
7. When the partitioning is complete, **FDISK** reboots your computer.
   Caution: Make sure to use the correct drive letters so that you do not format a drive that already contains data.
8. At the A: prompt, type **format c:/s**, where c is the letter of your first new partition, Repeat the format process for all the new partitions you have created.
9. After you format your DOM, it is ready to use.

Block Diagram



About Our Flash Management

In order to gain the best management for flash memory, PQI ***DiskOnModule*** supports an efficient and swift algorithm. Due to the life of flash memory is limited, PQI try to increase the life of our flash product through the following arrangement. There are some blocks are reserved in flash memory and these blocks would not be used in normal operation. Once any block is fail, one of these reserved blocks will replace it and the data of the fail block would be transferred to the reserved block for keeping the data's accuracy. After we used the above arrangement in flash memory, the life of the device will be longer than the device without it. When all of the reserved blocks have replaced the bad blocks, the device will be locked automatically to prevent programming, but the data can still be read out for back up.

Because the block of flash memory has a limited life, when the host writes data in the same address, PQI ***DiskOnModule*** does not to program data into the same physical place of the flash memory in purpose, our algorithm will get the data precisely when the host wants to read the data.

ECC (Error Correction Code) feature also be built in our hardware and firmware, it will correct 1 bit errors, and detect 2 bits errors when they happened. ECC ensured the accuracy of the data, and decreased the effect of the cross talking on the bus.

Pin Signal Assignment

The signals assigned for 44/40-pin applications are described in Table 1

Table 1 – Signal assignments for 44-pin ATA

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin) or Vcc
DMARQ	21	21	22	22	Ground
DIOW-	23	23	24	24	Ground
DIOR-	25	25	26	26	Ground
IORDY	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground
+5 V (logic) (see note)	41	41	42	42	+5 V (Motor) (see note)
Ground(return) (see note)	43	43	44	44	TYPE- (0=ATA) (see note)
NOTE – Pins which are additional to those of the 40-pin cable.					

Interface Signal Assignments And Descriptions

Signal summary

The physical interface consists of receivers and drivers communicating through a set of conductors using an asynchronous interface protocol. Table 2 defines the signal names.

Table 2 - Interface signal name assignments

Description	Host	Dir	Dev	Acronym
Cable select	(see note)			CSEL
Chip select0	→			CS0-
Chip select1	→			CS1-
Data bus bit 0 ~ Data Bus bit 15	⇔			DD0 ~ DD15
Device active or slave (Device 1) present	(see note)			DASP-
Device address bit 0	→			DA0
Device address bit 1	→			DA1
Device address bit 2	→			DA2
DMA acknowledge	→			DMACK-
DMA request	←			DMARQ
Interrupt request	←			INTRQ
I/O read	→			DIOR-
I/O ready	←			IORDY
I/O write	→			DIOW-
Passed diagnostics	(see note)			PDIAG-
Reset	→			RESET-
NOTE – See signal descriptions for information on source of these signals				

Signal Descriptions

CS0- (CHIP SELECT 0)

This is the chip select signal from the host used to select the Command Block registers.

CS1 – (CHIP SELECT 1)

This is the chip select signal from the host used to select the Control Block registers.

DA2, DA1, AND DA0 (DEVICE ADDRESS)

This is the 3-bit binary coded address asserted by the host to access a register or data port in the device.

DASP – (Device active, device 1 present)

This is a time-multiplexed signal which indicates that a device is active, or that Device 1 is present. This signal shall be an open collector output and each device shall have a 10 kΩ pull-up resistor.

If the host connects to the DASP- signal for the illumination of an LED or for any other purpose, the host shall ensure that the signal level seen on the ATA interface for DASP- shall maintain V_{OH} and V_{OL} compatibility, given the I_{OH} and I_{OL} requirements of the DASP- device drivers.

DD (15:0) (Device data)

This is an 8- or 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit register transfers.

DIOR- (Device I/O read)

This is the read strobe signal from the host. The falling edge of DIOR- enables data from the device onto the signals, DD (7:0) or DD (15:0). The rising edge of DIOR- latches data at the host and the host shall not act on the data until it is latched.

DIOW- (Device I/O write)

This is the Write strobe signal from the host. This rising edge of DIOW- latches data from the signals, DD (7:0) or DD (15:0), into the device. The device shall not act on the data until it is latched.

DMACK- (DMA acknowledge)

This signal shall be used by the host in response to DMARQ to initiate DMA transfers.

DMARQ (DMA request)

This signal, used for DMA data transfer between host and device, shall be asserted by the device when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK- i.e., the device shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.

This line shall be released (high impedance state) whenever the device is not selected or is selected and no DMA command is in progress. When enabled by DMA transfer, it shall be driven high and low by the device.

When a DMA operation is enabled, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.

INTRQ (Device interrupt)

This signal is used to interrupt the host system. INTRQ is asserted only when the device has a pending interrupt, the device is selected, and the host has cleared the nIEN bit in the Device Control register. If the nIEN bit is equal to one, or the device is not selected, this output is in a high impedance state, regardless of the presence or absence of pending interrupt.

The pending interrupt condition shall be set by:

- the completion of a command; or
- at the beginning of each data block to be transferred for PIO transfers except for the first data block for FORMAT TRACK. WRITE SECTOR(S), WRITE BUFFER, and WRITE LONG commands.

The pending interrupt condition shall be cleared by:

- assertion of RESET-; or
- the setting of the SRST bit of the Device Control register; or
- the host writing the Command register; or
- The host reading the Status register.

IOCS 16- (Device 16-bit I/O)

Obsolete.

IORDY (I/O channel ready)

This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.

If actively asserted, the signal only be enabled during DIOR-/DIOW- cycles to the selected device. If open collector, when IORDY is not negated, it shall be in the high-impedance (undriven) state.

This use of IORDY is required for PIO modes 3 and above and otherwise optional.

PDIAG - (Passed diagnostics)

This signal shall be asserted by Device 1 to indicate to Device 0 that it has completed diagnostics. A 10 kΩ pull-up resistor shall be used on this signal by each device.

The host shall not connect to the PDIAG-signal.

RESET- (Device reset)

This signal from the host system shall be asserted beginning with the application of power and held asserted until at least 25 μs after voltage levels have stabilized within tolerance during power on and negated thereafter unless some event requires that the device(s) be reset following power on.

ATA devices shall not recognize a signal assertion shorter than 20 ns valid reset signal. Devices may respond to any signal assertion greater than 20 ns, and shall recognize a signal equal to or greater than 25 μs.

CSEL (Cable select)

The device is configured as either Device 0 or Device 1 depending upon the value of CSEL.

Interface Register Definitions And Descriptions

Device addressing considerations

In traditional controller operation, only the selected device receives commands from the host following selection. In this standard, the register contents go to both devices (and their embedded controllers.) The host discriminates between the two by using the DEV bit in the Device/Head register.

Data is transferred in parallel either to or from host memory to the device's buffer under the direction of commands previously transferred from the host. The device performs all of the operations necessary to properly write data to, or read data from, the media. Data read from the media is stored in the device's buffer pending transfer to the host memory and data is transferred from the host memory to the device's buffer to be written to the media.

The devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two devices are daisychained on the interface, commands are written in parallel to both devices, and for all except the EXECUTE DEVICE DIAGNOSTICS command, only the selected device executes the command. On an EXECUTE DEVICE DIAGNOSTICS command addressed to Device 0, both devices shall execute the command, and Device 1 shall post its status to Device 0 via PDIAG-.

Devices are selected by the DEV bit in the Device/Head register. When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected. When devices are daisy chained, one shall be set as Device 0 and the other as Device 1.

I/O register descriptions

Communication to or from the device is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA (2:0), DIOR-, AND DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device. The Control Block Registers are used for device control and to post alternate status.

Anytime a command is in progress, that is, from the time the Command register is written until the device has completed the command and posted ending status, the device shall have either BSY or DRQ set to one. If the Command Block registers are read by the host when BSY or DRQ is set to one, the content of all register bits and fields except BSY and DRQ in the Status and Alternate Status registers is indeterminate. If the host writes to any Command Block register when BSY or DRQ is set to one, the results are indeterminate and may result in the command in progress ending with a command abort error.

When performing PIO transfers, BSY and DRQ shall both be cleared to zero within 400 ns of the transfer of the final byte of data. This assertion signals the completion of a PIO data transfer command.

Table 3 lists these registers and the addresses that select them.

Table 3 - I/O port functions and selection address

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
N	N	×	×	×	Data bus high impedance	Note used
					Control block registers	
N	A	0	×	×	Data bus high impedance	Note used
N	A	1	0	×	Data bus high impedance	Note used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	(see note1)	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number LBA (7:0) (see note 2)	Sector Number LBA (7:0) (see note 2)
A	N	1	0	0	Cylinder Low LBA (15:8) (see note 2)	Cylinder Low LBA (15:8) (see note 2)
A	N	1	0	1	Cylinder High LBA (23:16) (see note 2)	Cylinder High LBA (23:16) (see note 2)
A	N	1	1	0	Device/Head LBA (27:24) (see note 2)	Device/Head LBA (27:24) (see note 2)
A	N	1	1	1	Status	Command
A	A	×	×	×	Invalid address	Invalid address

Key:
A = signal asserted, N = signal negated, × = don't care
NOTES_
1 This register is obsolete. It is recommended that a device not respond to a read of this address. If a device does respond, it shall not drive the DD7 signal to prevent possible conflict with floppy disk implementations.
2 Mapping of registers in LBA translation.

Each register description in the following clauses contain the following format:

ADDRESS – the CS and DA address of the register.

DIRECTION – indicates if the register is read/write, read only, or write only from the host.

ACCESS RESTRICTIONS – indicates when the register may be accessed.

EFFECT – indicates the effect of accessing the register.

FUNCTIONAL DESCRIPTION – describes the function of the register.

FIELD/BIT DESCRIPTION – describes the content of the register.

[Duplicate Data, Error and Feature register]

During word access, the address space occupied by the Data Register interferes with the space occupied by the Error register and Feature register, and reference cannot be made to these registers. Therefore, the PC Card ATA Standard provides an area where the copy of each register does not duplicate in the contiguous I/O mode and memory map mode. The even-numbered address of the data register is provided in the offset "08h", and the odd-numbered address of the data register is located in the offset "09h". The copy of Error/Feature register is provided at the ODh.

Duplicate Data register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data Word															
Odd Data Byte Only								Even or Even-Odd Data Byte							

Duplicate registers Access

Data register	CE2#	CE#	A0	Offset	Data Bus
Word Data register	0	0	0	0h,8h	D15-D0
Word Data register	0	0	1	1h,9h	D15-D0
Even Byte Data register	1	0	0	0h,8h	D7-D0
Odd Byte Data register	1	0	1	9h	D7-D0
Odd Byte Data register	0	1	×	8h,9h	D15-D8
Error/Feature register	1	0	1	1h,0Dh	D7-D0
Error/Feature register	0	1	×	0h,1h	D15-D8
Error/Feature register	0	0	×	0Ch,0Dh	D15-D8

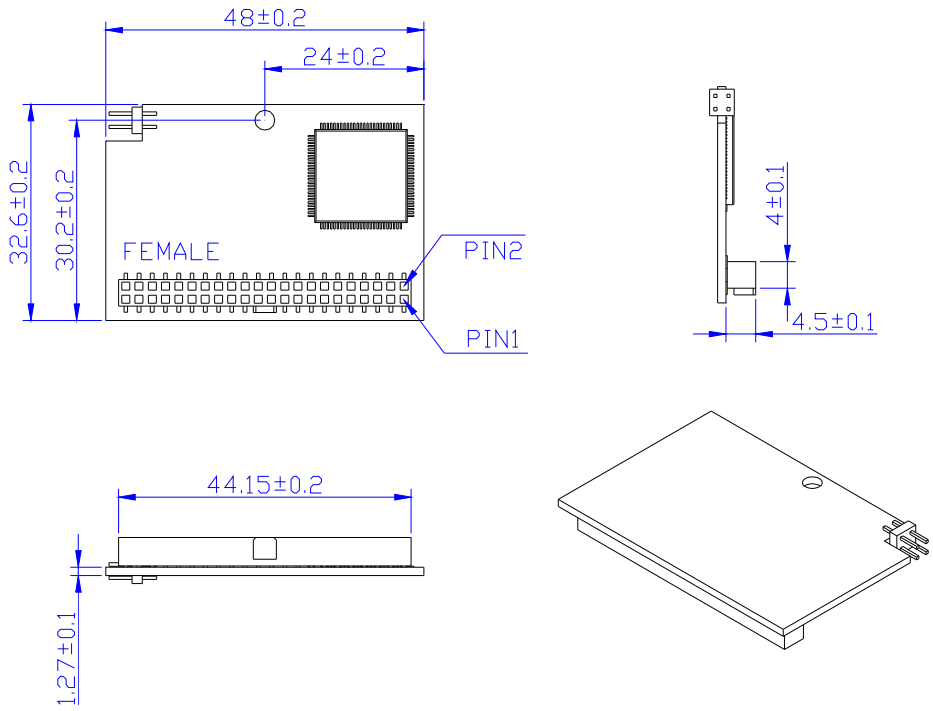
Initial value of task file register

After resetting and execution of the Execute Device Diagnostic command, the task file register is initialized as follows:

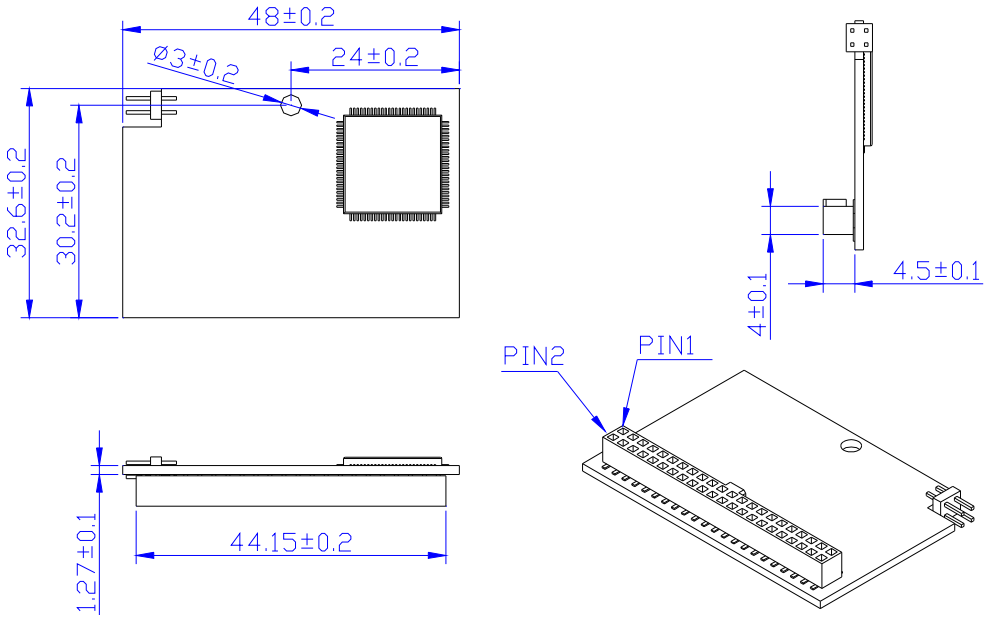
Sector Count register	01h
Sector Number register	01h
Cylinder Lo register	00h
Cylinder High register	00h
Device/Head register	A0h

Physical Outline

DH0XXXX44NX1 (44 PIN)



DH0XXXX44NX2 (44 PIN)



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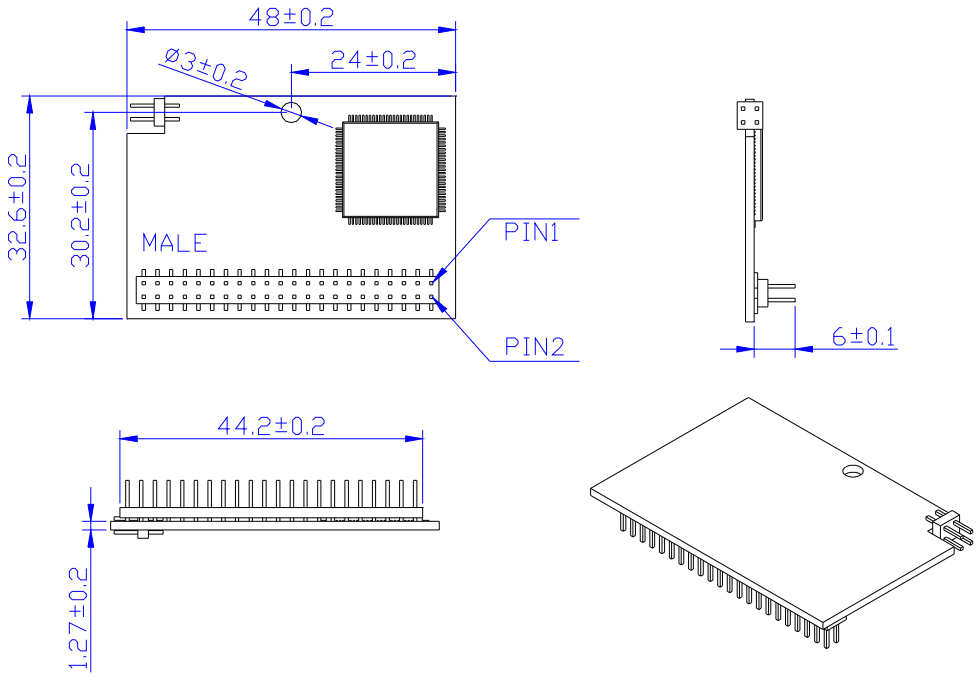
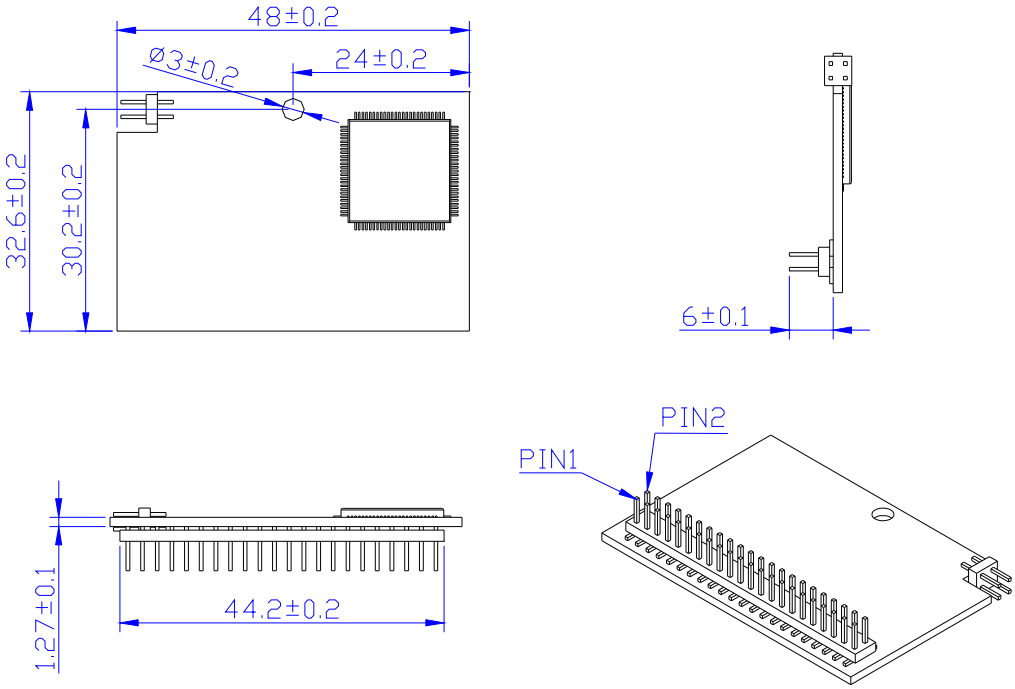
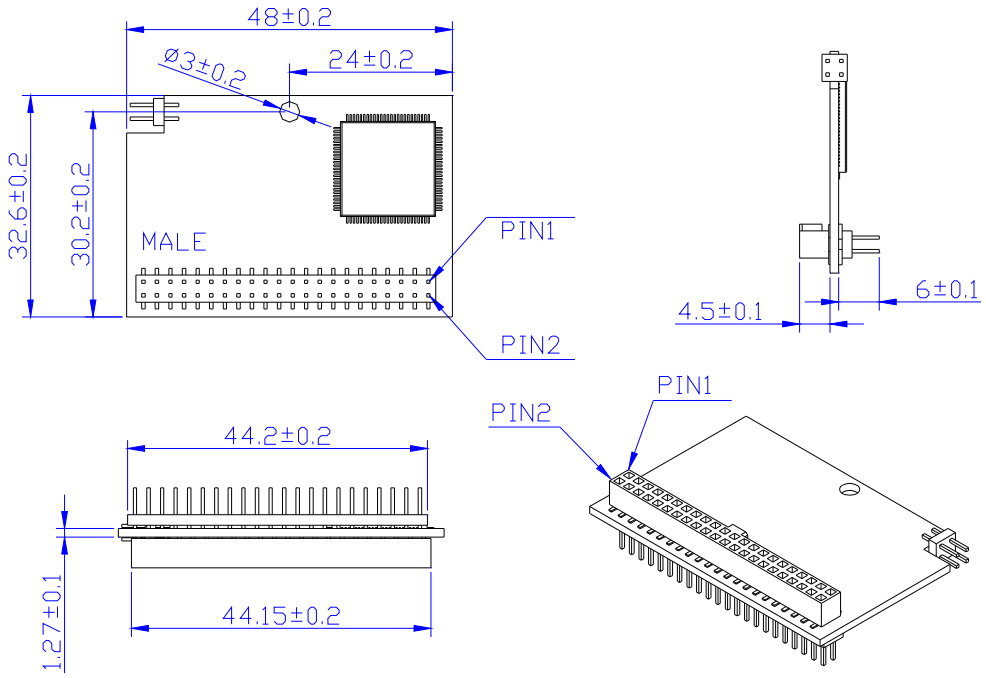


DH0XXXX44NX4 (44 PIN)



DH0XXXX44NX5 (44 PIN)



DH0XXXX44NX6 (44 PIN)