

DATA SHEET

Industrial CompactFlash Card



AC31-XXXX-XXX1

AC31-XXXX-XXX2

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1. Description

AC31-XXXX is **CompactFlash™** based on TDK GBDriver flash memory controller technology. This card complies with **CompactFlash™** specification, it is suitable for the usage of data storage memory for PC or other electric equipment and digital still camera. This card is equipped with NAND flash memory. By using this card it is possible to operate stability for the system that have **CompactFlash™** slots.

Fixed mode (045A)~AC31-XXXX-XXX2 disk use in system storage, some operating system can not accept boot-up from removable mode (848A)~AC31-XXXX-XXX1 disk like windows XP, when we boot-up from CFC with windows XP, the system detect the device will disable Removable device boot-up function, so the system can not finish the boot-up process. For this issue, we can setting the device mode to Fixed mode (045A) to solve this problem.

The CFC setting to Fixed or Removable mode will no any function different or issue.

2. Features

- 32Mbytes~2Gbytes flash memory card.
- **CompactFlash™** specification: PCMCIA ver.2.1 and PC Card ATA ver.2.01 compatible 50pin SMT connector and type I (3.3mm).
- 3.3V/5V single power supply operation.
- Internal self-diagnostic program operates at VCC power on.
- 3 variations of access mode:
 - Memory Card Mode.
 - I/O Card Mode.
 - True-IDE Mode.
- High reliability based on internal ECC (Error Correcting Code) Function.
- Data reliability is 1 error in 10^{14} bits read.
- Temperature range: 0 to +70 .
- MTBF: 1,000,000 hours.
- Endurance: 2,000,000 erase/program cycles
- Power Consumption (3.3V/ 5.0V).
 - Active mode: 24.1mA/ 26.5mA (3.3v/ 5.0v).
 - Sleep mode: 200 uA / 300 uA (3.3v/ 5.0v).
- High Performance:
 - Read: 4.0Mbytes/s.(32Mbytes~64Mbytes) , 4.1Mbytes/s.(128Mbytes~2Gbytes)
 - Write: 1.5Mbytes/s.(32Mbytes~64Mbytes) , 3.5Mbytes/s.(128Mbytes~2Gbytes)

Notes: The performance will depend on different platform with different test result.

3. Interface Description

3.1 Card pin Assignment

Pin NO.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	I/O	Signal name	I/O	Signal name	I/O
1	GND	-	GND	-	GND	-
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1		-CE1		-CE1	
8	A10		A10		A10	
9	-OE		-OE		-ATASEL	
10	A9		A9		A9	
11	A8		A8		A8	
12	A7		A7		A7	
13	VCC	-	VCC	-	VCC	-
14	A6		A6		A6	
15	A5		A5		A5	
16	A4		A4		A4	
17	A3		A3		A3	
18	A2		A2		A2	
19	A1		A1		A1	
20	A0		A0		A0	
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOIS16	O	-IOIS16	O
25	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	-CE2		-CE2		-CE2	
33	-VS1	O	-VS1	O	-VS1	O
34	-IORD		-IORD		-IORD	
35	-IOWR		-IOWR		-IOWR	
36	-WE		-WE		-WE	
37	RDY/-BSY	O	-IREQ	O	INTRQ	O
38	VCC	—	VCC	—	VCC	—
39	-CSEL		-CSEL		-CSEL	
40	-VS2	O	-VS2	O	-VS2	O
41	RESET		RESET		-RESET	
42	-WAIT	O	-WAIT	O	IORDY	O
43	-INPACK	O	-INPACK	O	-INPACK	O
44	-REG		-REG		-REG	
45	BVD2	I/O	-SPKR	I/O	-DASP	I/O
46	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	—	GND	—	GND	—

3.2 Card pin Description

Signal Name	Dir	Pin No.	Description
A10 to A0 (PC Card Memory Mode)	I	8,10,11,12,14,15,16,17,18,19,20	These address lines along with the-REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF + Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card , a byte in the card's information structure and its configuration control and status registers.
A10 to A0 (PC Card I/O Mode)			
A2 to A0 (True IDE Mode)		18,19,20	In True IDE Mode only A {2:0} are used to select the one of eight registers in the Task File. The remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as BVD1 is not supported
-STSCHG (PC Card Memory Mode)			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states; while the I/O interface is configured. Its use is controlled by the Card Configured and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card / I/O Mode)			This line is the Binary AUDIO OUTPUT FROM THE CARD .if the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave
-CD1,-CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompcatFlash Storage Card or CF + Card. They are used by the host to determine that the CompactFlash Storage Card or CF +Card is fully inserted into its socket.
-CE1,-CE2 (PC Card I/O Mode)	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A1.-CE1,-CE2 allows 8 bit hosts to access all data on D0 to D7. See Access specification below.
-CE1,-CE2 (PC Card I/O Mode)			
-CS0,-CS1 (True IDE Mode)			
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pins is open, this device is configured as a Slave.
-CSEL (True IDE Mode)			



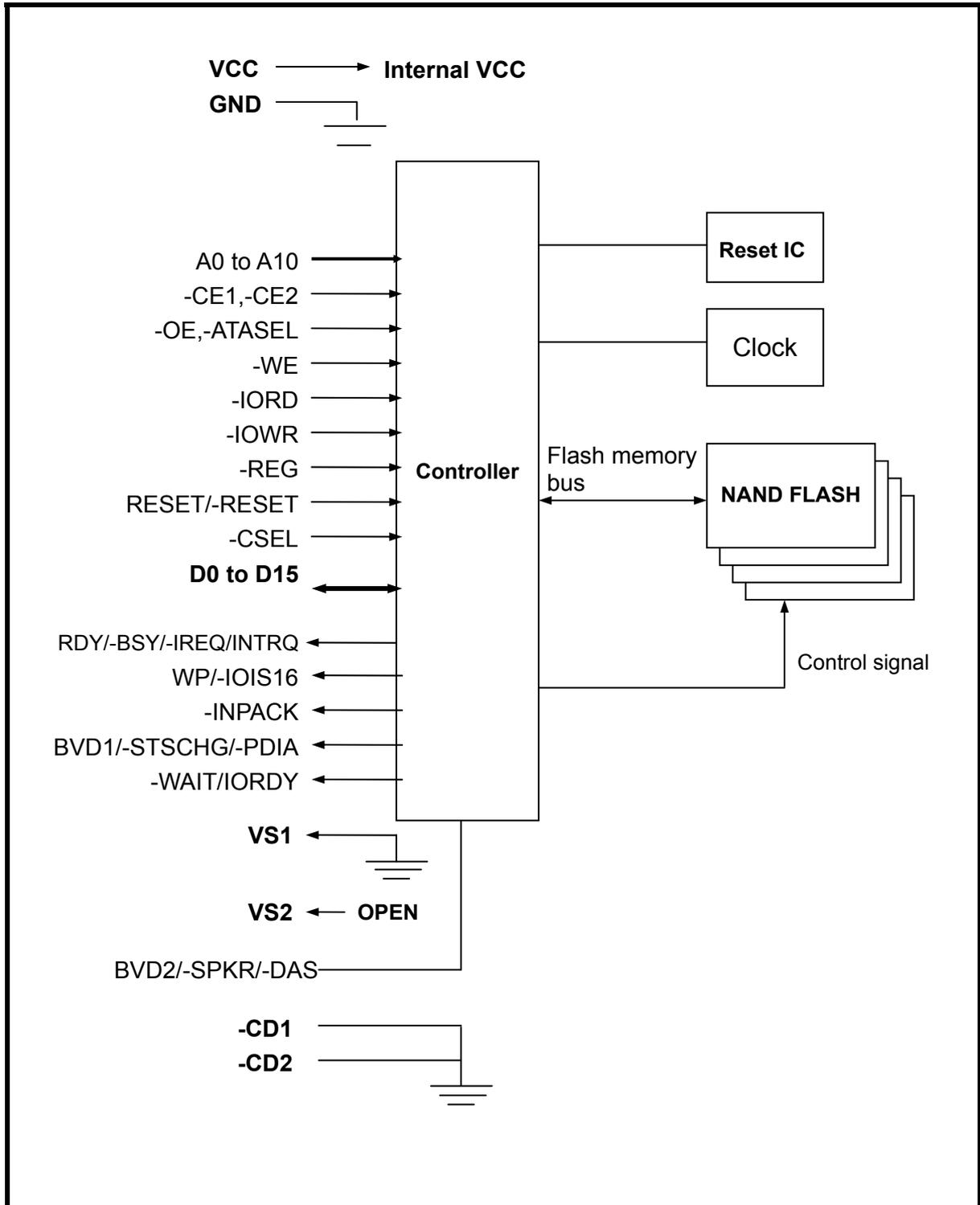
Signal Name	Dir	Pin No.	Description
D15 to D00 (PC Card Memory Mode)	I/O	31,30,29,28,27,49,48,47,6,5,4,3,223,22,21	These lines carry the Data, Commands and Status information between the host and the controller.D00 is the LSB of the Even Byte of the Word.D08 is the LSB of the Even Byte of the Word.D08 is the LSB of the Odd Byte of the Word. True IDE Mode, all Task File operations occur in byte mode on the low order bus D00 to D07 while all data transfers are 16 bit using D00 to D15.
D15 to D00 (PC Card I/O Mode)			
D15 to D00 (True IDE Mode)			
GND (PC Card Memory Mode)	-	1,50	Ground
GND (PC Card I/O Mode)			
GND (True IDE Mode)			
-INPCAK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode)			The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF +Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF +Card and the CPU.
-INPACK (True IDE Mode)			In True IDE Mode this output signal is not used and should not be connected at the host.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF +Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has same function as in PC Card I/O Mode.
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompcatFlash Storage Card or CF +Card controller registers when the CompactFlash Storage Card or CF +Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (Trailing edge)
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Signal Name	Dir	Pin No.	Description
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF +Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode. This signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
RDY/BSY (PC Card Memory Mode)	O	37	In Memory Mode this signal is set high when the CompactFlash Storage Card or CF +Card is ready to accept a new data transfer operation and held low when the card is busy . The Host memory card socket must provide a pull-up resistor. At power up and at Reset the RDY/-BSY signal is held low (busy) until the CompactFlash Storage Card or CF +Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF +Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true. The CompactFlash Storage Card or CF +Card has been powered up with + RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)			Operation-After the CompactFlash Storage Card or CF + Card has been configured for I/O operation; this signal is used as interrupt Request. This line is strobe low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high interrupt Request to the host.
-REG (PC Card Memory Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register(Attribute) Memory accesses. High for Common Memory. Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-REG (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
RESET (PC Card Memory Mode)	I	41	When the pin is high, this signal Resets the CompactFlash Storage Card or CF +Card. The CompactFlash Storage Card or CF +Card is Reset only at power up if this pin is left high or open from power-up. The CompactFlash Storage Card or CF +Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset form the host.

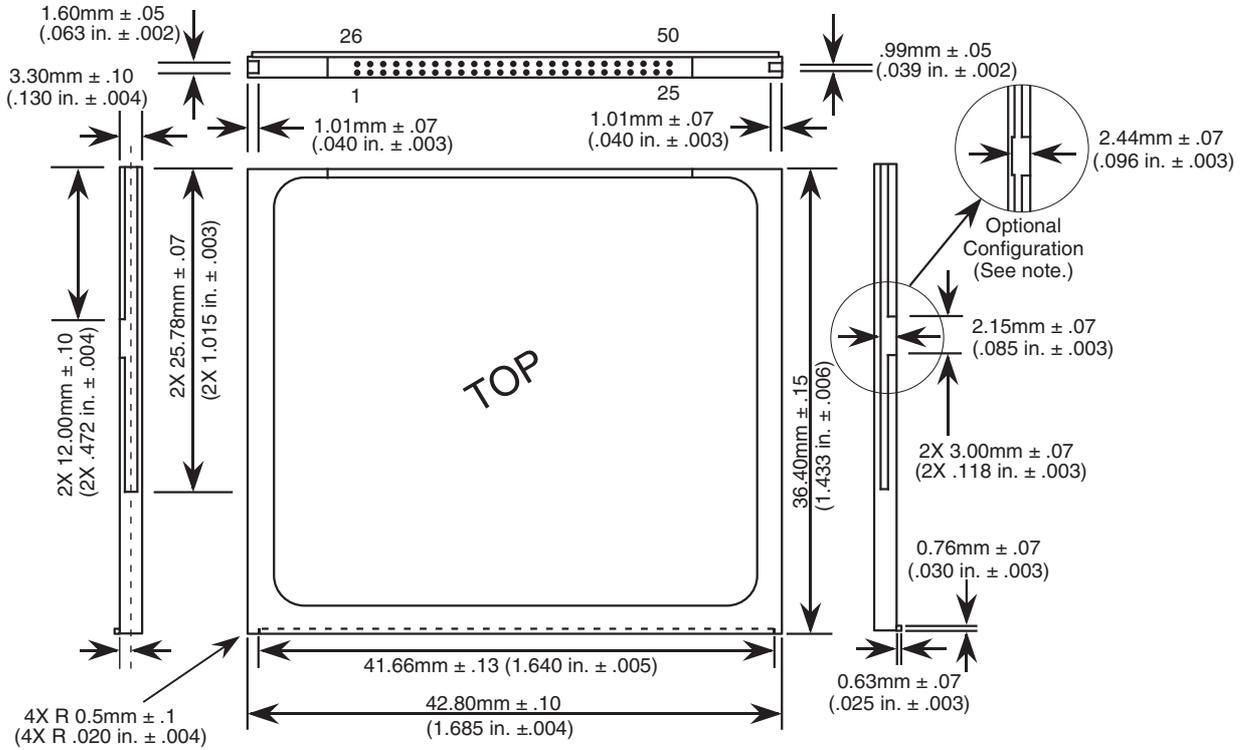


Signal Name	Dir	Pin No.	Description
VCC (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	—	13,38	+5V +3.3V power.
-VS1 /-VS2 (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	O	33,40	Voltage Sense Signals. -VS1 is grounded so that the CompactFlash Storage Card or CF + Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage.
-WAIT (PC Card Memory Mode)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card or CF + Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
IORDY (True IDE Mode)			In True IDE Mode this output signal may be used as IORDY
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for starting memory write data to the registers of the CompactFlash Storage Card or CF + Card when the card is configured I the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	24	Memory Mode-The CompactFlash Storage Card or CF + Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation-When the CompactFlash Storage Card or CF + Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16)function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

3.3 Card Block Diagram



4. Physical outline



Note: The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.