

F&eIT Series

RS-232C(2ch)

Communication Module

COM-2(FIT)GY

User's Manual

CONTEC CO.,LTD.

Check Your Package

Thank you for purchasing the CONTEC product.

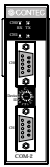
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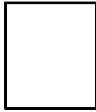
Product Configuration List

- Module[COM-2(FIT)GY] ...1
- First step guide ...1
- CD-ROM [F&eIT Series Setup Disk] *1 ...1

*1 The CD-ROM contains various software and User's Manual (this manual)



Module



First step guide



CD-ROM
[F&eIT Series Setup Disk]

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1. Introduction

This chapter provides information you should know before using the product.

About the modules

The COM-2(FIT)GY, which performs serial data transfers to and from an external device, can be used as an expansion port for the F&eIT series microcontroller unit.

The module can also serve as an expansion COM port for a media converter [RP-COM(FIT)H, RP-COM(FIT)H-AF, FX-DS540-COM2].

By reading this manual carefully, please build a system by creating applications programs, setting the switches, and connecting the module to external devices.

Features

- The COM-2(FIT)GY is equipped with two channels of RS-232C-compliant serial I/O ports.
- High-speed communication is supported at up to 921,600bps (115,200bps in compatible mode).
- A baud rate can be set by software.
- The module has 128-byte FIFO buffers for transmit and receive.
- Driver software is supplied to allow the serial ports to be used as standard Windows or Linux COM ports. *1
- It corresponds to both the compatible and enhanced mode and when an enhanced mode is selected, it is possible to use it by occupying the one interrupt level per one unit.
- Up to three units can be added (at the time of enhanced mode) as expansion ports for micro controller unit. *2
- Up to three units can be added as expansion ports for media converters [RP-COM(FIT)H, RP-COM(FIT)H-AF, FX-DS540-COM2].
- Similar to other F&eIT series products, the system, in the module itself, incorporates a 35mm DIN rail mounting mechanism as a standard item. A connection to a controller module can be effected on a lateral, stack basis in a unique configuration, which permits a simple, smart system configuration without the need for a backplane board.

*1: When using it as the expansion port for micro controller unit

*2: One unit can be added at the time of compatible mode

Customer Support

CONTEC provides the following support services for you to use CONTEC products more efficiently and comfortably.

Web Site

Japanese <http://www.contec.co.jp/>
English <http://www.contec.com/>
Chinese <http://www.contec.com.cn/>

Latest product information

CONTEC provides up-to-date information on products.
CONTEC also provides product manuals and various technical documents in the PDF.

Free download

You can download updated driver software and differential files as well as sample programs available in several languages.

Note! For product information

Contact your retailer if you have any technical question about a CONTEC product or need its price, delivery time, or estimate information.

Limited One-Year Warranty

CONTEC F&EIT products are warranted by CONTEC CO., LTD. to be free from defects in material and workmanship for up to one year from the date of purchase by the original purchaser.

Repair will be free of charge only when this device is returned freight prepaid with a copy of the original invoice and a Return Merchandise Authorization to the distributor or the CONTEC group office, from which it was purchased.

This warranty is not applicable for scratches or normal wear, but only for the electronic circuitry and original products. The warranty is not applicable if the device has been tampered with or damaged through abuse, mistreatment, neglect, or unreasonable use, or if the original invoice is not included, in which case repairs will be considered beyond the warranty policy.

How to Obtain Service

For replacement or repair, return the device freight prepaid, with a copy of the original invoice. Please obtain a Return Merchandise Authorization number (RMA) from the CONTEC group office where you purchased before returning any product.

* No product will be accepted by the CONTEC group without the RMA number.

Liability

The obligation of the warrantor is solely to repair or replace the product. In no event will the warrantor be liable for any incidental or consequential damages due to such defect or consequences that arise from inexperienced usage, misuse, or malfunction of this device.

Safety Precautions

Understand the following definitions and precautions to use the product safely.

Safety Information

This document provides safety information using the following symbols to prevent accidents resulting in injury or death and the destruction of equipment and resources. Understand the meanings of these labels to operate the equipment safely.

⚠ DANGER	DANGER indicates an imminently hazardous situation which, if not avoided, will result in death or serious injury.
⚠ WARNING	WARNING indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.
⚠ CAUTION	CAUTION indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury or in property damage.

Handling Precautions

⚠ CAUTION

- Do not modify the module. CONTEC will bear no responsibility for any problems, etc., resulting from modifying this module.
- Do not use or store the equipment in a hot or cold place, or in a place that is subject to severe temperature changes (Operating temperature range: 0 - 50°C).
- Do not use or store the equipment in a place subject to direct sunlight or near a heating device, such as a stove.
- Do not use or store the equipment in a dusty or humid place.
(Operating humidity range: 10 - 90%RH, No condensation)
- As this product contains precision electronic components, do not use or store in environments subject to shock or vibration.
- Do not use or store the product near equipment generating a strong magnetic field or radio waves.
- If you notice any strange odor or overheating, please unplug the power cord immediately.
- In the event of an abnormal condition or malfunction, please consult the dealer from whom the equipment was purchased.
- To avoid electric shock, please do not touch the system with a wet hand.
- Do not open the module casing. CONTEC will disclaim any responsibility for equipment whose casing has been opened.
- To prevent damage, please do not subject the module to impact or bend it.
- To prevent contact malfunction, please do not touch the metallic pins on the external module connector.

- The module contains switches that need to be properly set. Before using the module, please check its switch settings.
 - To avoid malfunction, please do not change the module switch settings in an unauthorized manner.
 - Do not operate the device module when the power for the Controller Module is on.
To avoid malfunction, please be sure to turn off the power for the Controller Module.
-

FCC PART 15 Class A Notice

NOTE

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in commercial environment.

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference at his own expense.

WARNING TO USER

Change or modifications not expressly approved the manufacturer can void the user's authority to operate this equipment.

Environment

Use this product in the following environment. If used in an unauthorized environment, the module may overheat, malfunction, or cause a failure.

Operating temperature

0 - 50°C

Humidity

10 - 90%RH (No condensation)

Corrosive gases

None

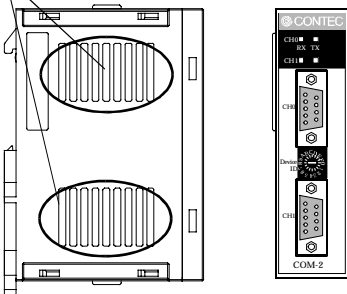
Floating dust particles

Not to be excessive

Inspection

Inspect the product periodically as follows to use it safely.

*The ventilation slits are not covered,
and neither dust nor alien substance is
attached to the ventilation slits



Storage

When storing this product, keep it in its original packing form.

- (1) Put the module in the storage bag.
- (2) Wrap it in the packing material, then put it in the box.
- (3) Store the package at room temperature at a place free from direct sunlight, moisture, shock, vibration, magnetism, and static electricity.

Disposal

When disposing of the product, follow the disposal procedures stipulated under the relevant laws and municipal ordinances.

2. Module Nomenclature and Settings

Nomenclature of Module Components

Figure 2.1 shows the names of module components.

In the figure, the indicated switch settings represent factory settings.

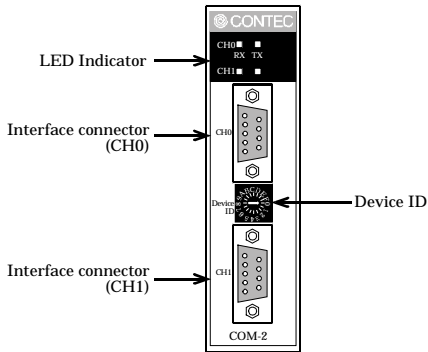


Figure 2.1. Names of Module Components

Setting a Device ID

Depending on the specific Device ID that is set, the COM-2(FIT)GY can be switched over between the compatible mode and the enhanced mode. Table 2.1 shows the relationship between Device IDs and the modes. For a description of the compatible and enhanced modes, see Chapter 6, "Using the Module".

The factory setting is [0], in which the COM-2(FIT)GY can be used as a COM3/COM4 standard port.

⚠ CAUTION

This document describes the setting method for combination with a microcontroller. For combination with a media converter, read the manual for the media converter carefully before making any settings.

Setup Method

A Device ID can be set by turning the rotary switch on the device face.

To set a Device ID, turn the switch knob.



Figure 2.2. Setting a Device ID

Table 2.1. I/O Address

ID No.	CH0		CH1		Mode
	I/O address (h)	Interrupt level	I/O address (h)	Interrupt level	
0	03E8 - 03EF	IRQ5	02E8 - 02EF	IRQ7	Compatible (COM3/4)
1	03E8 - 03EF	IRQ5	02E8 - 02EF	Not used	Compatible (COM3/4)
2	03E8 - 03EF	Not used	02E8 - 02EF	IRQ7	Compatible (COM3/4)
3	03E8 - 03EF	Not used	02E8 - 02EF	Not used	Compatible (COM3/4)
4	01A0 - 01A7	IRQ5	01A8 - 01AF	IRQ5	Enhanced
5	01A0 - 01A7	IRQ7	01A8 - 01AF	IRQ7	Enhanced
6	02A0 - 02A7	IRQ5	02A8 - 02AF	IRQ5	Enhanced
7	02A0 - 02A7	IRQ7	02A8 - 02AF	IRQ7	Enhanced
8	9800 - 9807	IRQ9	9808 - 980F	IRQ9	Enhanced
9	9820 - 9827	IRQ5	9828 - 982F	IRQ7	Enhanced
A	9840 - 9847	IRQ7	9848 - 984F	IRQ9	Enhanced
B	9860 - 9867	Not used	9868 - 986F	Not used	Enhanced
C	0700 - 0707	IRQ9	0708 - 070F	IRQ9	Enhanced
D	0720 - 0727	IRQ7	0728 - 072F	IRQ7	Enhanced
E	Reserved	Reserved	Reserved	Reserved	Reserved
F	Reserved	Reserved	Reserved	Reserved	Reserved

⚠ CAUTION

When using the product in the Windows environment, select a Device ID No. other than 8, 9, A and B.

LED Indicator

- RX: Indicates that the module is receiving serial data (green).
TX: Indicates that the module is transmitting serial data (green).

3. Connecting to an External Device

Interface Connector

How to Connect an Interface Connector

The interface connector that is provided on the module can be used to connect the module to an external device.

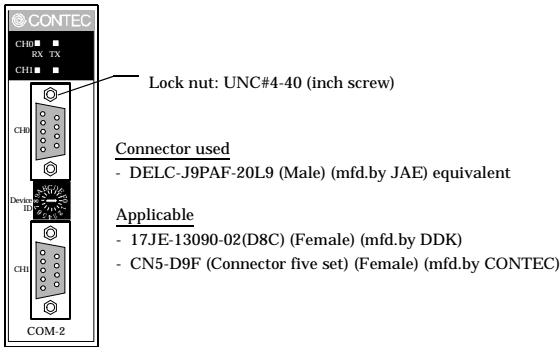


Figure 3.1. The Interface Connector, and Connectors That Can Be Used

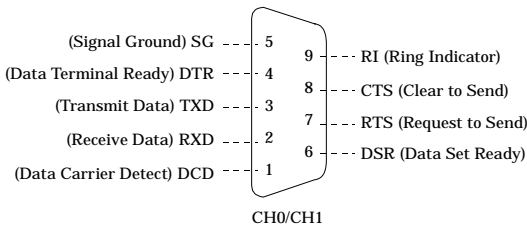


Figure 3.2. Signal Layout on the Interface Connector

Cable Connection

The RS-232C interface may require different cables, depending upon the specific device, such as a modem or a computer (personal computer) to which a connection is established. When selecting a cable, check the specifications for the external device to be connected, and select either a straight cable or a crossed (reversed cable), depending on the type of the device to be connected. If signal lines must be rearranged within a connector, appropriate action should be taken according to the required specifications.

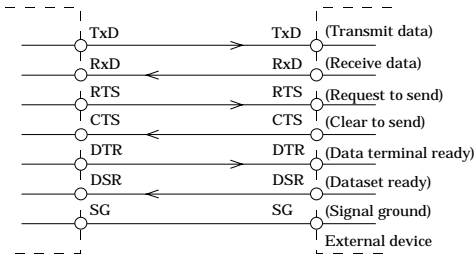


Figure 3.3. Connecting to a Modem

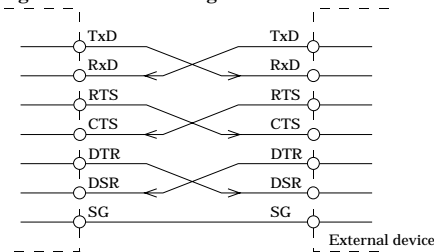


Figure 3.4. Connecting to a Personal Computer

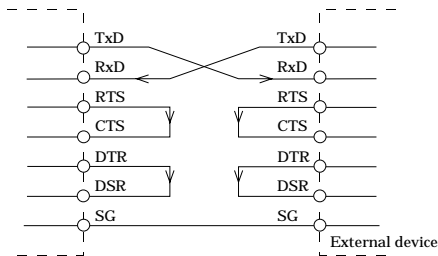


Figure 3.5. Connecting to a Device

⚠ CAUTION

The connecting device and this module may cause malfunction when connecting it with the wrong wire,

4. Functions

This section describes the functions of the module.

Communication Function

Serial Data Transmission

Sends and receives data in accordance with the RS-232C standard.

Baud rates can be selected from 2 - 921,600bps bps by means of software.

Send and Receive Data Buffers

The module has a separate 128-byte send and 128-byte receive buffer.

The buffers operate as FIFO buffers and help reduce the load on the CPU for high-speed communications or system operation.

The FIFO trigger size is a data buffer size that determines the timing of generating a hardware interrupt.

Increasing the FIFO trigger size decreases the number of times hardware interrupts occur for data transmission and reception, thereby reducing the load on the CPU.

However, this delays the timing of transmitting data to the remote device and the timing of notifying an application of data reception because actual transmission and reception take place after a certain amount of data has been collected.

In contrast, decreasing the FIFO trigger size or disabling FIFO memory shortens the timing of data transmission and reception but may increase the load on the CPU or miss some receiving data.

Since the FIFO trigger size is variable, adjusting it depending on the system results in optimum performance.

Setting the Baud Rate

The output baud rate can be set by setting the appropriate value to the Baud Rate Generator register. The available setting range depends on which clock mode is used.

Clock 3 mode: 15 - 921,600bps

Clock 2 mode: 8 - 460,800bps

Clock 1 mode: 4 - 230,400bps

Clock 0 mode: 2 - 115,200bps

However, some baud rate values do not have a corresponding Baud Rate Generator register setting. If the result of substituting the baud rate into the equation below is an integer, then that baud rate can be set. If the result contains a fractional part, the baud rate cannot be set.

Clock 3 mode

$921600 \div \text{Desired baud rate} = \text{Division register setting value}$

Ex.) $921600 \div 9600\text{bps} = 96$ (As the result is an integer, this baud rate can be set.)

$921600 \div 128000\text{bps} = 7.2$ (As the result contains a fractional part, this baud rate cannot be set.)

Clock 2 mode

$460800 \div \text{Desired baud rate} = \text{Division register setting value}$

Ex.) $460800 \div 9600\text{bps} = 48$ (As the result is an integer, this baud rate can be set.)

$460800 \div 128000\text{bps} = 3.6$ (As the result contains a fractional part, this baud rate cannot be set.)

Clock 1 mode

$230400 \div \text{Desired baud rate} = \text{Division register setting value}$

Ex.) $230400 \div 9600\text{bps} = 24$ (As the result is an integer, this baud rate can be set.)

$230400 \div 128000\text{bps} = 1.8$ (As the result contains a fractional part, this baud rate cannot be set.)

Clock 0 mode

$115200 \div \text{Desired baud rate} = \text{Division register setting value}$

Ex.) $115200 \div 9600\text{bps} = 12$ (As the result is an integer, this baud rate can be set.)

$115200 \div 76800\text{bps} = 1.5$ (As the result contains a fractional part, this baud rate cannot be set.)



CAUTION

See Chapter 5 “Interrupt Vector Registers” for selecting the clock frequency (1.8432, 3.6864, 7.3728, or 14.7456 MHz).

For use in compatible mode, clock 0 (1.8432 MHz) is used as a fixed setting.

Refer to the following baud rate setting examples. Baud rates other than those listed below can also be set if they produce a valid setting value in the equation described above.

Table 4.1. Baud Rate Generator Programming Table

Output baud rate	Clock 0 mode (1.8432MHz)		Clock 1 mode (3.6864MHz)		Clock 2 mode (7.3728MHz)		Clock 3 mode (14.7456MHz)	
	Baud Rate Generator register	Setup error (%)	Baud Rate Generator register	Setup error (%)	Baud Rate Generator register	Setup error (%)	Baud Rate Generator register	Setup error (%)
2	57600	-						
4	28800	-	57600	-				
5	23040	-	46080	-				
8	14400	-	28800	-	57600	-		
15	7680	-	15360	-	30720	-	61440	-
50	2304	-	4608	-	9216	-	18432	-
75	1536	-	3072	-	6144	-	12288	-
110	1047	0.026	2094	0.026	4189	0.0022	8378	0.0022
134.5	857	0.058	1713	0.0006	3426	0.0006	6852	0.0006
150	768	-	1536	-	3072	-	6144	-
300	384	-	768	-	1536	-	3072	-
600	192	-	384	-	768	-	1536	-
1200	96	-	192	-	384	-	768	-
1800	64	-	128	-	256	-	512	-
2000	58	0.68	115	0.17	230	0.17	461	0.04
2400	48	-	96	-	192	-	384	-
3600	32	-	64	-	128	-	256	-
4800	24	-	48	-	96	-	192	-
7200	16	-	32	-	64	-	128	-
9600	12	-	24	-	48	-	96	-
14400	8	-	16	-	32	-	64	-
19200	6	-	12	-	24	-	48	-
28800	4	-	8	-	16	-	32	-
38400	3	-	6	-	12	-	24	-
57600	2	-	4	-	8	-	16	-
76800			3	-	6	-	12	-
115200	1	-	2	-	4	-	8	-
153600					3	-	6	-
230400			1	-	2	-	4	-
460800					1	-	2	-
921600							1	-

5. Using the Module

Compatible and Enhanced Modes

The COM-2(FIT)GY can operate in two modes: the compatible mode, in which the COM-2(FIT)GY, when connected to CONTEC's microcontroller unit, acts as a standard serial port; and the enhanced mode, in which the COM-2(FIT)GY operates under CONTEC's unique control method. Before building a system using the COM-2(FIT)GY, a working understanding of the features of these modes may be in order.

- * To use four or more channels of COM in the Windows environment, select the enhanced mode, and then use the COM-DRV(W32) driver. (Ex.: Device ID-No. 04h, 07h, 0Ch)

Compatible Mode

The COM-2(FIT)GY can use two channels as standard serial ports.

Channels CH0 of the COM-2(FIT)GY can be assigned to COM3, and CH1 to COM4.

In the compatible mode, the COM-2(FIT)GY uses one interrupt level per channel.

When adding two channels, you need to ensure that at least two interrupt levels are available. For I/O addresses, the addresses that are assigned to the standard serial ports can be used. Because these addresses can be treated as standard serial ports, they can be accessed by using commonly available driver software that can handle standard serial ports.

Enhanced Mode

The enhanced mode operates the COM-2(FIT)GY by using CONTEC's unique control method.

The enhanced mode controls two channels at one interrupt level. Therefore, the channels can be operated even when only one interrupt level is available. For I/O addresses, CONTEC-designated addresses must be used.

When the COM-DRV(W32) driver is used, it can be used in the same way as a standard serial port.

Table 5.1. I/O Address

ID No.	CH0			CH1		
	Function	I/O address (h)	Interrupt level	Function	I/O address (h)	Interrupt level
0	COM3	03E8 - 03EF	IRQ5	COM4	02E8 - 02EF	IRQ7
1	COM3	03E8 - 03EF	IRQ5	COM4	02E8 - 02EF	Not used
2	COM3	03E8 - 03EF	Not used	COM4	02E8 - 02EF	IRQ7
3	COM3	03E8 - 03EF	Not used	COM4	02E8 - 02EF	Not used
4	Enhanced	01A0 - 01A7	IRQ5	Enhanced	01A8 - 01AF	IRQ5
5	Enhanced	01A0 - 01A7	IRQ7	Enhanced	01A8 - 01AF	IRQ7
6	Enhanced	02A0 - 02A7	IRQ5	Enhanced	02A8 - 02AF	IRQ5
7	Enhanced	02A0 - 02A7	IRQ7	Enhanced	02A8 - 02AF	IRQ7
8	Enhanced	9800 - 9807	IRQ9	Enhanced	9808 - 980F	IRQ9
9	Enhanced	9820 - 9827	IRQ5	Enhanced	9828 - 982F	IRQ7
A	Enhanced	9840 - 9847	IRQ7	Enhanced	9848 - 984F	IRQ9
B	Enhanced	9860 - 9867	Not used	Enhanced	9868 - 986F	Not used
C	Enhanced	0700 - 0707	IRQ9	Enhanced	0708 - 070F	IRQ9
D	Enhanced	0720 - 0727	IRQ7	Enhanced	0728 - 072F	IRQ7
E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

**CAUTION**

Please use it excluding Device ID No. 8, 9, A, B when using in the Windows environment.

Operating under CPU-SB303-FIT

When using the module under CONTEC's microcontroller unit CPU-SB303-FIT, the OS must be set to recognize the I/O address and interrupt level used by the COM-2(FIT)GY. In CPU-SB303-FIT, this is called hardware installation. Use the following installation procedure.

Compatible Mode Installation Procedure

- (1) Do not connect COM-2(FIT)GY to CPU-SB303-FIT. Turn on the CPU-SB303-FIT.
- (2) Select [Start] from [Control Panel] and start the [Add Hardware].
- (3) Click [Next >] in response to [Welcome to the Add Hardware Wizard] in the Add Hardware Wizard.
- (4) Select the [Yes] from the [Has the hardware already been connected with the computer?] screen, and click [Next].
- (5) The next, select [Add a New Device] in response to [Choose a Hardware Task] and click [Next].
- (6) Select [No, select from a list [Advanced]] in response to [Do you want Windows to search for your new hardware?], and click [Next].
- (7) Select the [Ports (COM & LPT)] folder from the [Hardware types:] screen.
- (8) Select [Communications Port] from [Standard Types], and press [Next].
- (9) On the [Start Hardware Installation] screen, press [Next].
- (10) [Code 34] occurs in the [Completing the Add Hardware Wizard] screen, as resources are not assigned properly. To assign resources appropriately, select [View or change resources for this hardware (Advanced)].
- (11) On the [Properties] screen of [Add New Hardware Wizard], press the [Set Configuration Manually] to specify an I/O address and interrupt level.
- (12) Change [Base Configuration] and select an available I/O address. Then press [IRQ] to specify IRQ. Make sure that [Conflict information] is set to [No devices are conflicting].
- (13) Make sure that [Conflicting device list] is set to [No conflicts].
 - * Set the I/O address and interrupt level in the same way as for DeviceID. For details, see Table 5.1.
- (14) Press [Complete] to end the wizard.
- (15) The message [Do you want to restart now?] will appear. Select [Yes] to restart the OS.
- (16) Once the operation is completed according to the instructions, the installation will be completed. When using more than one unit in Compatible Mode, repeat (2) - (15).
- (17) Set DeviceID according to the I/O address and interrupt level registered in the system.
- (18) Always make sure that CPU-SB303-FIT is turned off, when connecting COM-2(FIT)GY to CPU-SB303-FIT.

(19) Turn on CPU-SB303-FIT to start the OS. This completes the installation. After the completion of the installation, always check the resources, using the [How to Verify Resources Managed by OS] section as a reference.

Enhanced Mode Installation Procedure

When it is used with Enhanced Mode, COM driver of the bundled CD-ROM is necessary.

Refer to “COMDRV(W32)Main_e.html” being attached to the bundled CD-ROM for the way of installing it.



CAUTION

When used in Enhanced Mode, the product cannot be used with Device ID 4 or 5. To use the product in Enhanced Mode, select another Device ID.

How to Verify Resources Managed by OS

Always check the PC resources (I/O address and interrupt level) assigned to the COM-2(FIT)GY before actually using this product. Use the following procedure to check the resources managed by the OS.

- (1) Select [System] from [Control Panel] and click [Hardware] property sheet, then open [Device Manager].
- (2) For Compatible mode, double click on the [Ports (COM & LPT)] folder. For Enhanced mode, double click on the [Multi-function adapters] folder.
- (3) Double click on the [CONTEC CO., LTD. - COM-2(FIT)GY] or [COM*] folder to display the properties screen.
- (4) Select [Resources]. Check the resource items and settings, and look for any conflicts.
- (5) If changing an I/O address, change the Basic configuration from the [Setting based on:]. To change an interrupt level, click on [Change setting (C)].

After checking the resources, check again that the interrupt level value on the COM-2(FIT)GY match the settings in the OS.

I/O Ports and Registers

The module uses the XR16C2850 (Exar Corporation) upward compatible with the 16550 UART.

For details on the internal registers of the XR16C2850 and its control, refer to the XR16C2850 data sheet.

In enhanced mode, “starting I/O address + 1Fh” is used as an interrupt vector register.

I/O Ports

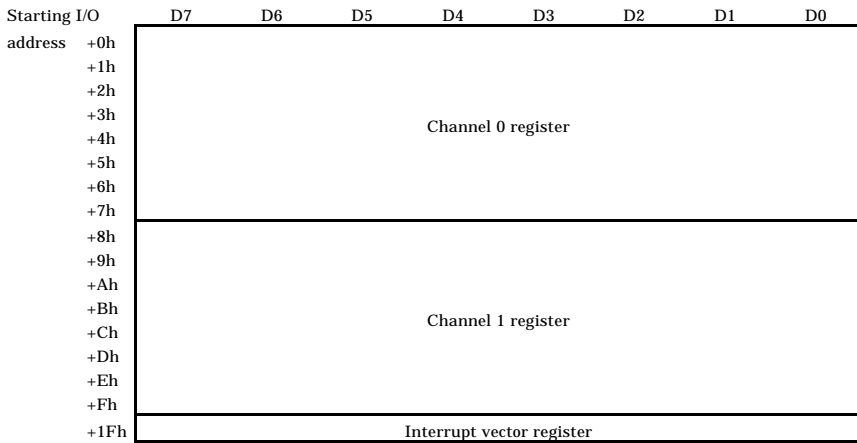


Figure 5.1. I/O Ports



CAUTION

Each port must be accessed in bytes to conform to device specifications.

Non-byte access to any port is not allowed (such as word access or doubleword access).

Details on I/O Ports and Registers

The XR16C2850's internal registers are port-mapped differently depending on the value set in the Line Control Register (LCR).

The General Registers are enabled at startup or with LCR Bit 7 = 0 and LCR = other than 0xBFh.

The Baud Rate Registers are enabled with LCR Bit 7 = 1.

The Enhanced Registers are enabled with LCR = 0xBFh.

Input port 1 (General Registers)

Starting I/O address	D7	D6	D5	D4	D3	D2	D1	D0
+0h/+8h	Receive Holding Register (RHR)							
	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
+1h/+9h	Interrupt Enable Register (IER)							
	CTS Interrupt (*2)	RTS Interrupt (*2)	Xoff Interrupt (*2)	Sleep Mode (*2)	MODEM Status Interrupt	Receive Line Status Interrupt	Transmit Holding Register	Receive Holding Register
+2h/+Ah	Interrupt Status Register (ISR)							
	FIFOs Enable	FIFOs Enable	-RTS, -CTS	Xoff	Int Priority Bit 2	Int Priority Bit 1	Int Priority Bit 0	Int Status
+3h/+Bh	Line Control Register (LCR)							
	Divisor Latch Enable	Set Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit 1	Word Length Bit 0
+4h/+Ch	Modem Control Register (MCR)							
	Clock Prescaler Select (*2)	IR Mode Enable (*2)	Xon Any (*2)	Loop Back Enable	-OP2 and INT Enable	Out 1 0:INT Enable 1:INT Disable (*1)	-RTS	-DTR
+5h/+Dh	Line Status Register (LSR)							
	FIFO Error	THR& TSR Empty	THR Empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Receive Data Ready
+6h/+Eh	Modem Status Register (MSR)							
	-CD	-RI	-DSR	-CTS	Delta -CD	Delta -RI	Delta -DSR	Data -CTS
+7h/+Fh	Scratch Pad Register (SPR)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
+7h/+Fh	FIFO Level Counter (FLVL) (*3)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*1 For details, see the "Using an Interrupt" section.

*2 These bits are enabled with EFR Bit 4 = 1.

*3 These registers are enabled with FCTR Bit 6 = 1.

Figure 5.2. Input port (General Registers)

Input port 2 (Baud Rate Registers)

Starting I/O	D7	D6	D5	D4	D3	D2	D1	D0
address +0h/+8h	LSB of Divisor Latch (DLL)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
+1h/+9h	MSB of Divisor Latch (DLM)							
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Figure 5.3. Input port (Baud Rate Registers)

Input port 3 (Enhanced Registers)

Starting I/O	D7	D6	D5	D4	D3	D2	D1	D0
address +0h/+8h	FIFO Level Counter							
	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC
+1h/+9h	Feature Control Register (FCTR)							
	Rx/Tx Mode	SCPAD Swap	Trig Bit 1	Trig Bit 0	RS485 Auto control	IrRx Inv.	-RTS Delay Bit 1	-RTS Delay Bit 0
	Enhanced Feature Register (EFR)							
+2h/+Ah	Auto -CTS	Auto -RTS	Special Char, select	Enable IER Bits 4-7, ISR, FCR Bits 4-5, MCR Bits 5-7	Cont-3 Tx, Rx Control	Cont-2 Tx, Rx Control	Cont-1 Tx, Rx Control	Cont-0 Tx, Rx Control
	Xon-1 Word							
+4h/+Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Xon-2 Word							
+5h/+Dh	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	Xoff-1 Word							
+6h/+Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Xoff-2 Word							
+7h/+Fh	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Figure 5.4. Input port (Enhanced Registers)

Input port 4 (Interrupt vector register)

Starting I/O	D7	D6	D5	D4	D3	D2	D1	D0
address +1Fh	Interrupt vector register							
	Fixed at "0"	(Reserved)					CH1 Interrupt	CH0 Interrupt

Figure 5.5. Input port (Interrupt vector register)

Output port 1 (General Registers)

Starting I/O address	D7	D6	D5	D4	D3	D2	D1	D0
+0h/+8h	Transmit Holding Register (THR)							
	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
+1h/+9h	Interrupt Enable Register (IER)							
	CTS Interrupt (*2)	RTS Interrupt (*2)	Xoff Interrupt (*2)	Sleep Mode (*2)	MODEM Status Interrupt	Receive Line Status Interrupt	Transmit Holding Register	Receive Holding Register
+2h/+Ah	FIFO Control Register (FCR)							
	RCVR	RCVR	TX Trigger (MSB)	TX Trigger (LSB)	DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enable
+3h/+Bh	Line Control Register (LCR)							
	Divisor Latch Enable	Set Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit 1	Word Length Bit 0
+4h/+Ch	Modem Control Register (MCR)							
	Clock Prescaler Select (*2)	IR Mode Enable (*2)	Xon Any (*2)	Loop Back Enable	-OP2 and INT Enable	Out 1 0:INT Enable 1:INT Disable (*1)	-RTS	-DTR
+5h/+Dh	Disable							
+6h/+Eh	Disable							
+7h/+Fh	Scratch Pad Register (SPR)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
+7h/+Fh	Enhanced Mode Select Registers (EMSR) (*3)							
	Reserved	Reserved	RTS Hyst Bit 3	RTS Hyst Bit 2	Reserved	Reserved	Alt.RX/TX FIFO Count	RX/TX FIFO Count

*1 For details, see the "Using an Interrupt" section.

*2 These bits are enabled with EFR Bit 4 = 1.

*3 These registers are enabled with FCTR Bit 6 = 1.

Figure 5.6. Output port (General Registers)

Output port 2 (Baud Rate Registers)

Starting I/O address	D7	D6	D5	D4	D3	D2	D1	D0
+0h/+8h	LSB of Divisor Latch (DLL)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
+1h/+9h	MSB of Divisor Latch (DLM)							
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Figure 5.7. Output port (Baud Rate Registers)

Output port 3 (Enhanced Registers)

Starting I/O address	D7	D6	D5	D4	D3	D2	D1	D0
+0h/+8h	FIFO Level Counter							
	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC	Trig/FC
+1h/+9h	Feature Control Register (FCTR)							
	Rx/Tx Mode	SCPAD Swap	Trig Bit 1	Trig Bit 0	RS485 Auto control	IrRx Inv.	-RTS Delay Bit 1	-RTS Delay Bit 0
+2h/+Ah	Enhanced Feature Register (EFR)							
	Auto -CTS	Auto -RTS	Special Char. select	Enable IER Bits 4-7, ISR, FCR Bits 4-5, MCR Bits 5-7	Cont-3 Tx, Rx Control	Cont-2 Tx, Rx Control	Cont-1 Tx, Rx Control	Cont-0 Tx, Rx Control
+4h/+Ch	Xon-1 Word							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
+5h/+Dh	Xon-2 Word							
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
+6h/+Eh	Xoff-1 Word							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
+7h/+Fh	Xoff-2 Word							
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Figure 5.8. Output port (Enhanced Register)

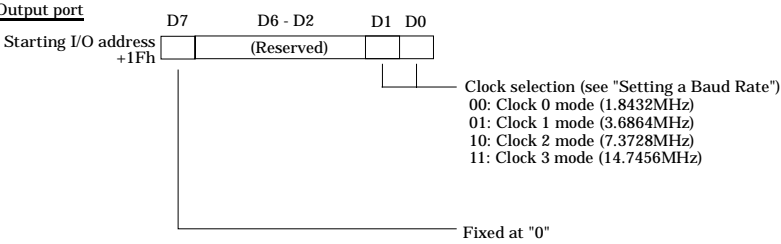
Output port 4 (Interrupt Vector Registers)

Starting I/O address	D7	D6	D5	D4	D3	D2	D1	D0
+1Fh	Interrupt vector register							
	Fixed at "0"	(Reserved)					Clock selection Bit 1	Clock selection Bit 0

Figure 5.9. Output port (Interrupt Vector Registers)

Interrupt Vector Registers

Output port



Input port

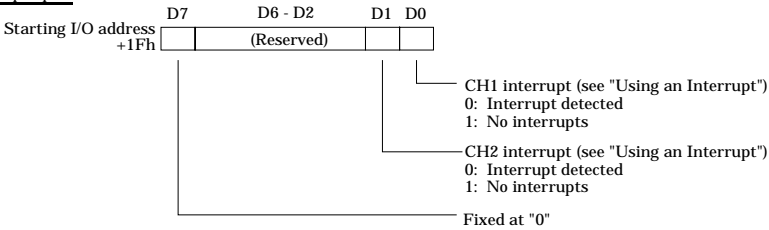


Figure 5.10. Interrupt Vector Registers

Using an Interrupt

Compatible Mode

When the Module is operated in the compatible mode, channels CH0 and CH1 are assigned to standard I/O addresses COM3 and COM4, respectively. The interrupt levels will be IRQ5 for CH0 and IRQ7 for CH1.

Enhanced Mode

When the Module is operated in the enhanced mode, 2-channel interrupts can be accepted only on a single interrupt request line. Individual channel interrupts can be checked on the interrupt vector register (IVR) when a specific interrupt is generated. Which interrupt line is used can be specified by means of Device ID switches.

When an interrupt is received, on what channel the interrupt occurred can be checked by reading the IVR within an interrupt service routine. When the interrupt service is executed, before exiting from the interrupt service, you need to re-read the IVR to check to see if there are any interrupts that are pending.

The XR16C2850 contains an internal register to enable itself for interrupts (make them available) or to check whether any interrupt has been generated. For using the register, refer to the data sheet for the XR16C2850 supplied by Exar Corporation.

For setting to use interrupts, use the D2 bit in the modem control register (MCR).

D2 bit of MCR	Write 0 : Enable (when the power is turned on)
	Write 1 : Disable

Examples

Following is a COM-2(FIT)GY sample program.

The program involves sending and receiving data through channels CH0 and CH1. When the Module is used in the compatible mode or the module is to be connected to a remote device, the cable must be connected as illustrated in the figure below. When the Module is operated in the enhanced mode, a cross cable must be used as illustrated in the figure below.

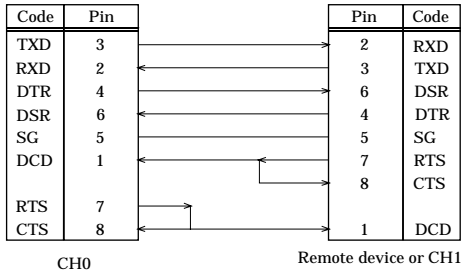


Figure 5.11. Cable Connection Diagram

Compatible Mode

Flowchart

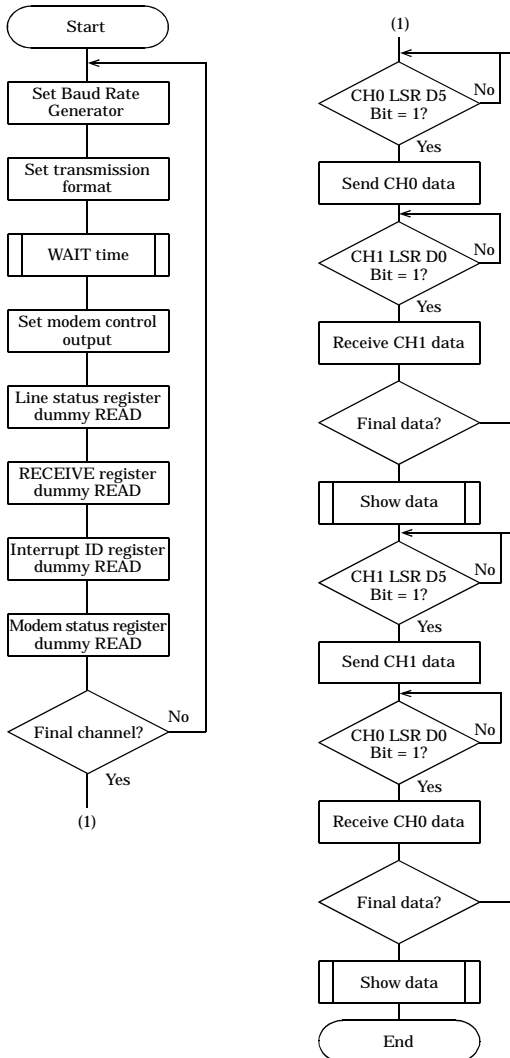


Figure 5.12. Flow chart (Compatible mode)

Sample Program

```

/*=====
=
  Sample program 1    -- CH0 <=> CH1 Loop Test --

      DEVICE ID:      0
      Mode:           Compatible Mode
      Channel 0:      03E8H (COM3)
      Channel 1:      02E8H (COM4)
      Baud Rate:      115,200 bps
      Interrupt:      N/A

=====
*/
#include <stdio.h>
#include <conio.h>

/* ----- Constant ----- */
#define CH      2                /* no. of channels */
#define NUM     10               /* data of total number */
#define BPS     1                /* baud rate */

      unsigned char  rbuf[CH][NUM];                /* receive buffer */
      unsigned int  ADR[CH] = {0x3e8, 0x2e8}; /* I/O address */
      unsigned int  rcnt[CH] = {0, 0};            /* receive count */

/* ----- Prototype -----
*/
void main( void );

/* ----- Main -----
*/
void main( void )
{
  unsigned char  i, j;
  int            dummy;

  for(i = 0; i < CH; i ++ ) {                /* RS-232C initialize */
    outp( ADR[i]+0x3, 0x80 );                /* Line Control Register (DLAB SET) */
    outp( ADR[i]+0x0, BPS & 0xff ); /* Divisor Latch (Baud Rate SET) */
    outp( ADR[i]+0x1, (BPS >> 8) & 0xff );
    outp( ADR[i]+0x3, 0x0 );                /* Line Control Register (DLAB RESET) */

    outp( ADR[i]+0x3, 0x7 );                /* Line Control Register */
                                          /* ( Bit 0,1 ... Word Length = 8 bit )
*/
                                          /* ( Bit 2 ..... 2 stop bit          )
*/
    for(j = 0; j < 10; j++)                /* hardware wait */
      dummy = inp( 0x2ef );

    outp( ADR[i]+0x4, 0x3 );                /* MODEM Control Register (DTR . RTS) */
    dummy = inp( ADR[i]+0x5 );                /* Line Status Register(Dummy Read) */
    dummy = inp( ADR[i]+0x0 );                /* Receiver Buffer Register (Dummy Read)
*/
    dummy = inp( ADR[i]+0x2 );                /* Interrupt ID. Register (Dummy Read) */
    dummy = inp( ADR[i]+0x6 );                /* Modem Status Register (Dummy Read) */
    outp( ADR[i]+0x1, 0x1 );                /* Interrupt Enable Register */
  }
}

```

```

for(j = 0; j < NUM; j++) {
    while( !(inp( ADR[0]+0x5 ) & 0x20) ); /* transmitter empty */
    outp( ADR[0]+0x0, j );
    while( !(inp( ADR[1]+0x5 ) & 0x1) ); /* data ready */
    rbuf[1][rcnt[1]] = (unsigned char)inp( ADR[1]+0x0 );
    rcnt[1]++;
}
for(j = 0; j < NUM; j++) {
    printf(" CH0:%02x -> CH1:%02x ", j, rbuf[1][j]);
    if(rbuf[1][j] != j)printf("Verify Error \n"); /* verify data */
    else printf("\n");
}
printf("\n");

for(j = 0; j < NUM; j++) {
    while( !(inp( ADR[1]+0x5 ) & 0x20) ); /* transmitter empty */
    outp( ADR[1]+0x0, j );
    while( !(inp( ADR[0]+0x5 ) & 0x1) ); /* data ready */
    rbuf[0][rcnt[0]] = (unsigned char)inp( ADR[0]+0x0 );
    rcnt[0]++;
}
for(j = 0; j < NUM; j++) {
    printf(" CH1:%02x -> CH0:%02x ", j, rbuf[0][j]);
    if(rbuf[0][j] != j)printf("Verify Error \n"); /* verify data */
    else printf("\n");
}
}

/* ----- End of file -----
- */

```

Enhanced Mode

Flowchart

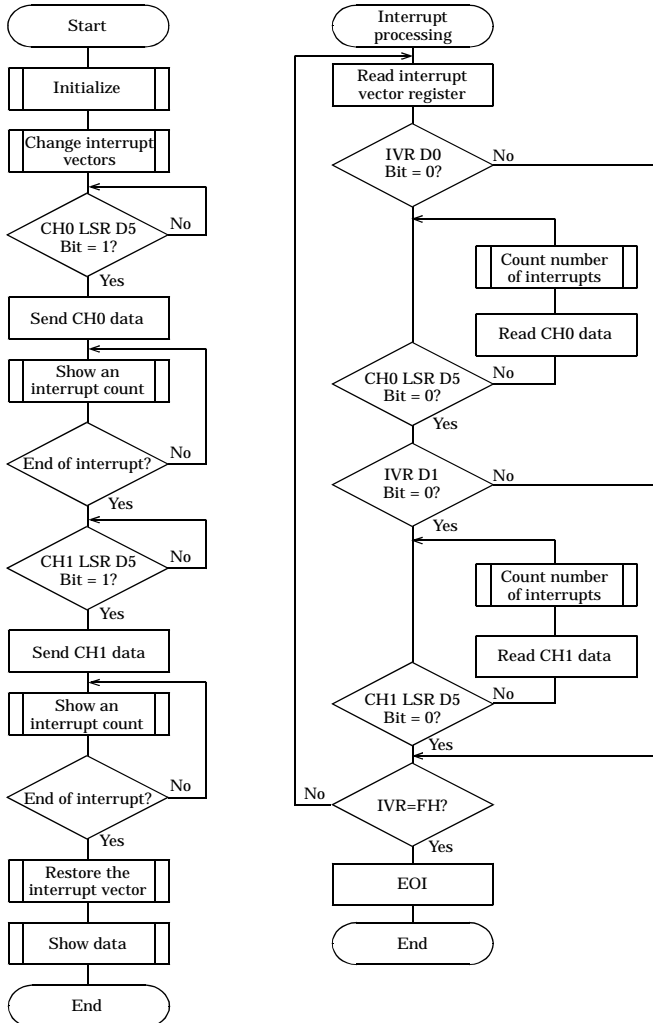


Figure 5.13. Flow chart (Enhanced mode)

Sample Program

```

/*
=====
Sample program 2  -- CH0 <=> CH1 Loop Test --

DEVICE ID:      4
Mode:           Enhanced Mode
Channel 0:      01A0H
Channel 1:      01A8H
Baud Rate:      115,200 bps
Interrupt:      IRQ5

=====
*/
#include <stdio.h>
#include <conio.h>
#include <dos.h>

/* ----- Constant ----- */
#define CH        2                /* no. of channels */
#define NUM       10               /* data of total number */
#define BPS       1                /* baud rate */
#define IRQ5      0                /* IRQ5 */
#define IRQ7      1                /* IRQ7 */

volatile unsigned char rbuf[CH][NUM]; /* receive buffer */
volatile unsigned int  ADR[CH] = {0x1a0, 0x1a8}; /* I/O address */
volatile unsigned int  intcnt[CH] = {0, 0}; /* interrupt counter */
volatile int           IrqLevel = IRQ5; /* interrupt level */
int                  OrgMasterImr; /* original IMR */
unsigned char IntVector[2] = { 0x0d, 0x0f }; /* interrupt vector */
unsigned char PicMask[2] = { 0xdf, 0x7f }; /* mask bit */
unsigned char IsrClear[3] = { 0x65, 0x67, 0x61 }; /* ISR clear */

/* ----- Prototype ----- */
void main( void );
void Initialize( void ); /* initialize */
void ChgVect( void ); /* change vector */
void ResVect( void ); /* restore vector */
void _interrupt _far inthandler( void ); /* interrupt handler */
void ( _interrupt _far *OrgVect )(); /* original vector */

/* ----- Initialize ----- */
void Initialize( void )
{
    unsigned int i, j;
    int dummy;

    for(i = 0; i < CH; i++) {
        outp( ADR[i]+0x3, 0x80 ); /* Line Control Register (DLAB SET) */
        outp( ADR[i]+0x0, BPS & 0xff ); /* Divisor Latch (Baud Rate SET) */
        outp( ADR[i]+0x1, (BPS >> 8) & 0xff );
        outp( ADR[i]+0x3, 0x0 ); /* Line Control Register (DLAB RESET) */
    }
}

```

```

        outp( ADR[i]+0x3, 0x7 );          /* Line Control Register */
                                        /* ( Bit 0,1 ... Word Length = 8 bit )
*/
                                        /* ( Bit 2 ..... 2 stop bit          )
*/
        for(j = 0; j < 10; j++)          /* hardware wait */
            dummy = inp( 0x2ef );

        outp( ADR[i]+0x4, 0x3 );          /* MODEM Control Register (DTR . RTS) */
        dummy = inp( ADR[i]+0x5 );        /* Line Status Register      (Dummy
Read) */
        dummy = inp( ADR[i]+0x0 );        /* Receiver Buffer Register (Dummy Read) */
        dummy = inp( ADR[i]+0x2 );        /* Interrupt ID Register (Dummy Read) */
        dummy = inp( ADR[i]+0x6 );        /* Modem Status Register (Dummy Read) */
        outp( ADR[i]+0x1, 0x1 );          /* Interrupt Enable Register */
    }
    outp( ADR[0]+0x1f, 0x80 );            /* Select Clock Mode */
}

/* ----- change vector -----
- */
void ChgVect( void )
{
    OrgVect = _dos_getvect( IntVector[IrqLevel] );
    _disable();
    _dos_setvect( IntVector[IrqLevel], inthandler );
    outp( 0x21, ( OrgMasterImr = inp( 0x21 ) ) & PicMask[IrqLevel] );
    outp( 0x20, IsrClear[IrqLevel] );     /* ISR clear */
    _enable();                             /* enable */
}

/* ----- restore vector -----
- */
void ResVect( void )
{
    _disable();                             /* disable */
    outp( 0x21, OrgMasterImr );
    _dos_setvect( IntVector[IrqLevel], OrgVect ); /* restore orgvect */
    _enable();                             /* enable */
}

/* ----- interrupt handler -----
- */
void _interrupt _far inthandler( void )
{
    unsigned char sts;

    _enable();                             /* enable */
    do {
        sts = (unsigned char)inp( ADR[0]+0x1f ); /* Int Vector Register */
        if( !(sts & 0x1) ) {                    /* CH0 status */
            while( inp( ADR[0]+0x05 ) & 0x1 ) {
                rbuf[0][intcnt[0]] = (unsigned char)inp( ADR[0]+0x0 );
                intcnt[0]++;                    /* count times of an interrupt */
            }
        }
        if( !(sts & 0x2) ) {                    /* CH1 status */
            while( inp( ADR[1]+0x05 ) & 0x1 ) {
                rbuf[1][intcnt[1]] = (unsigned char)inp( ADR[1]+0x0 );
                intcnt[1]++;                    /* count times of an interrupt */
            }
        }
    }
}

```

```

    }
  }
} while( !(sts & 0xf) );

_disable(); /* disable */
outp( 0x20, 0x20 ); /* EOI */
}

/* ----- main -----
*/
void main( void )
{
  unsigned int i, j;

  Initialize(); /* initialize */
  ChgVect(); /* change vector */

  for(j = 0; j < NUM; j++) { /* send CH0 to CH1 */
    while( !(inp( ADR[0]+0x5 ) & 0x20) ); /* transmitter empty */
    outp( ADR[0]+0x0, j );
  }
  while(intcnt[1] < 10)
    printf("Interrupt CH0:%02d CH1:%02d\n", intcnt[0], intcnt[1]);
  printf("\n");

  for(j = 0; j < NUM; j++) { /* send CH1 to CH0 */
    while( !(inp( ADR[1]+0x5 ) & 0x20) ); /* transmitter empty */
    outp( ADR[1]+0x0, j );
  }
  while(intcnt[0] < 10)
    printf("Interrupt CH0:%02d CH1:%02d\n", intcnt[0], intcnt[1]);
  printf("\n");

  ResVect(); /* restore vector */
  for(j = 0; j < NUM; j++) {
    printf(" CH0:%02x -> CH1:%02x ", j, rbuf[1][j]);
    if(rbuf[1][j] != j) printf("Verify Error \n"); /* verify data */
    else printf("\n");
  }
  printf("\n");
  for(j = 0; j < NUM; j++) {
    printf(" CH1:%02x -> CH0:%02x ", j, rbuf[0][j]);
    if(rbuf[0][j] != j) printf("Verify Error \n");
    else printf("\n");
  }
  printf("\n");
  printf("Interrupt CH0:%02d CH1:%02d\n", intcnt[0], intcnt[1]);
}

/* ----- End of file -----
- */

```


6. System Reference

Block Diagram

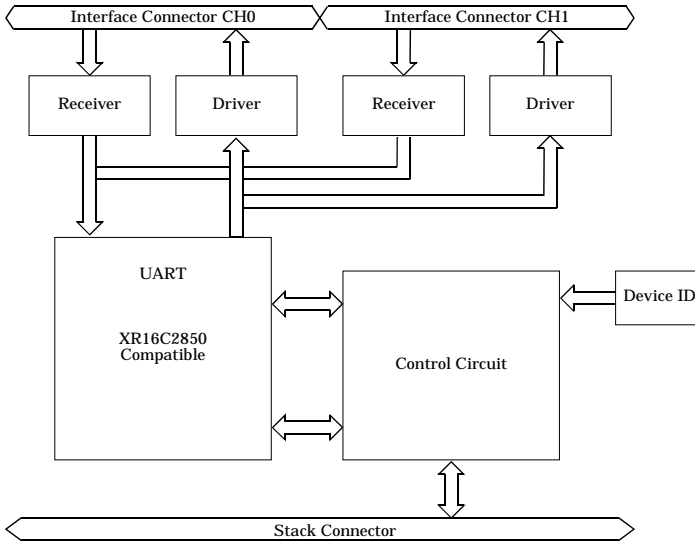


Figure 6.1. Block Diagram

Equivalence Circuit

MAX3245

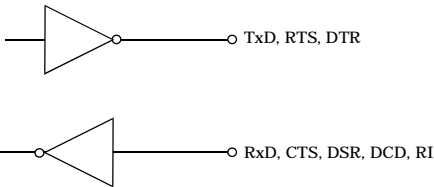


Figure 6.2. Equivalence Circuit

Specifications

Table 6.1. Specifications

Item	Specification
Number of channels	2ch
Interface type	RS-232C
Transfer method	Asynchronous serial transfer
Baud rate	2 - 921,600bps *1 *2
Data length	5, 6, 7, 8 bits 1, 1.5, 2 stop bits *1
Parity check	Even, Odd, Non-parity *1
Controller chip	162850 or equivalent (The module has 128-byte receive and 128-byte transmit FIFO buffers.)
Interrupt requests	1 or 2 level use
Power consumption	5VDC±5% 100mA (Max.)
Connecting distance	15m
Dimension (mm)	25.2(W) x 64.7(D) x 94.0(H) (exclusive of protrusions)
Weight(module itself)	100g
Module connection method	Stack connection by the connector that is provided with the side of module
Module installation method	One-touch connection to 35mm DIN rails. (standard connection mechanism provided in the system)

*1 These items can be set by software.

*2 Data transmission at high speed may not be performed normally depending on the environment including the type of status of connected material of cable and environment.

CAUTION

When connecting the module to a controller module, the internal power consumption should be taken into account. If the total current exceeds the capacity of the power supply unit, the integrity of the operation cannot be guaranteed. For further details, please see the Controller Module manual.

Table 6.2. Installation Environment Requirements

Parameter		Requirement description
Operating temperature		0 - 50°C
Storage temperature		-10 - 60°C
Humidity		10 - 90% (No condensation)
Floating dust particles		Not to be excessive
Corrosive gases		None
Line-Noise resistance	Line-noise	AC line/2kV, Signal line/1kV (IEC1000-4-4Level 3, EN61000-4-4Level 3)
	Static electricity resistance	Contact discharge/4kV (IEC1000-4-2Level 2, EN61000-4-2Level 2)
		Atmospheric discharge/8kV (IEC1000-4-2Level 3, EN61000-4-2Level 3)
Vibration resistance	Sweep resistance	10 - 57Hz/semi-amplitude 0.15mm, 57 - 150Hz/2.0G 80minutes each in X, Y, and Z directions (JIS C0040-compliant, IEC68-2-6-compliant)
	Impact resistance	15G, half-sine shock for 11ms in X, Y, and Z directions (JIS C0041-compliant, IEC68-2-27-compliant)

External Dimensions

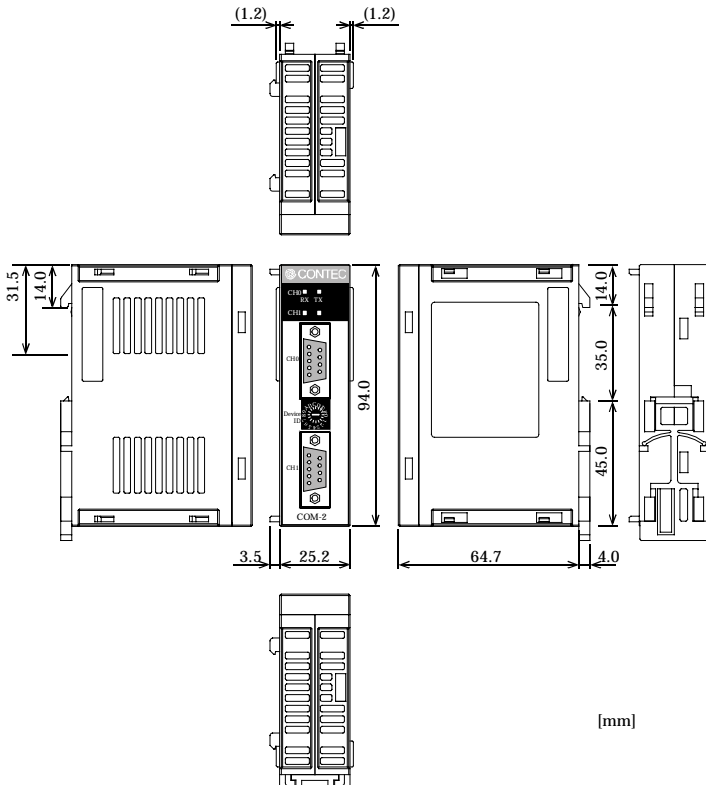


Figure 6.3. External Dimensions

COM-2(FIT)GY

User's Manual

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