AX10424

3 Channel Counter/Timer & 24 Bit DIO Module

User's Manual

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June 1994, 1st Edition

Printed in Taiwan

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Integrated circuits on computer boards are sensitive to static electricity. To avoid damaging chips from electrostatic discharge, observe the following precautions:

- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before handling a board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. This helps to discharge any static electricity on your body.
- Wear a wrist grounding strap, available from most electronic component stores, when handling boards and components.

Unpacking

The AX10424 is packed in an anti-static bag. The board has components that are easily damaged by static electricity. Do not remove the anti-static wrapping until proper precautions have been taken. Safety instructions in front of this User's Manual describe anti-static precautions and procedures.

Inventory and Inspection

After unpacking the board, place it on a raised surface and carefully inspect the board for any damage that might have occurred during shipment. Ground the board and exercise extreme care to prevent damage to the board from static electricity.

Integrated circuits will sometimes come out of their sockets during shipment. Examine all integrated circuits, particularly the BIOS, processor and keyboard controller chip to ensure that they are firmly seated.

The AX10424 3 Channel Counter/Timer & 24 Bit DIO Module package includes the following:

- **AX10424 Board**
- **Screw 3mm (x4)**
- **Bronze stick 6mm (x4)**
- **AS59099 DAC Driver CD**

Make sure that all of the items listed above are present.

What To Do If There Is A Problem

If there are damaged or missing parts, contact your supplier and/or dealer immediately. Do not attempt to apply power to the board if there is damage to any of its components.

Table of Contents

Chapter 1
Introduction

1.1 General Description

The AX10424 is a PC/104 module which is primary intended to PC embedded application in industrial environment. It contains 24 digital input/output channels and 3 counter/timer channels.

The 24-bit digital input and output are arranged to emulate 8255 PPI (Programmable Peripheral Interface) chip mode 0 but which stronger driving capability. The 24-bit DIO is further divided into three 8-bit ports (Port A, Port B and Port C) which can be functionally programmed as either digital input or digital output ports. There is a unique feature associated with AX10424. An external input interrupt ability. This feature frees up the PC to do other activities since there is no need to poll the digital input for an event to occur.

For timing functions, the AX10424 uses the popular 8254 integrate chip. The 8254 has three programmable counters and can be used as event counter, rate generator, square wave generator, frequency measurement, etc.

1.2 Applications

- Sense and control high level signals through I/O module.
- Sense low level (TTL) switches or signals.
- Drive indicator light or control recorders.
- Parallel data transfer to PC.
- Period and pulse width measurement.
- Event and frequency counting.
- Waveform and pulse generation.
- Baud rate generator

1.3 Features

- PC/104 standard expansions module.
- 24 TTL/DTL digital I/O lines.
- 24mA output drive/sink current.
- Easy interface to high level signals.
- Three 8-bit ports independently selectable for I/O.
- 3 programmable counter/timer channels.
- Include timed interrupt generation.
- 50-pin digital connector compatible with AX751, AX754, AX755, or AX756 accessory board.

1.4 Specifications

Digital I/O

- **Number of Channels :** *24*
- **I/O Configuration :** *TTL/DTL compatible*
- **Operation Mode :** *Emulates 8255 mode 0*
- **Input/Output Mode :** *Pair*
- **Improved Noise Margins :** *Hysteresis*

  $V_T+ - V_T- = 0.4(typ.)$
- **Added Pull-up Resistor :** *CMOS/dry contact compatible*
- **Digital Input**
  - Logic High Input Voltage : 2V min.
  - Logic Low Input Voltage : 0.8V max.
  - Logic High Input Current : 20uA max. at V_I = 2.7V
  - Logic Low Input Current : -0.2mA max. at V_{IL} = 0.4V
- **Digital Output**
  - Logic High Output Voltage : 2.4V min at I_{OH} = -3mA
  - Logic Low Output Voltage : 0.4V max at I_{OL} = 12mA
  - Logic High Output Current : -15mA source max.
  - Logic Low Output Current : 24mA sink max.

Programmable Counter/Timer

- **Type :** *82C54*
- **Number of Counters :** *3 independent 16-bit counters*
- **Frequency Range :** *DC to 10MHz*

- **Modes :** *6 programmable mode*
- **Input/Output Level :** *TTL; DTL; CMOS compatible*

Interrupt

- **PC bus IRQ :** *9(2), 5, 10, 11, 12, 15*
- **Source :** *Enable control and positive trigger*

Power Requirement

- **+5V :** *200mA typ.*

Physical/Environmental

- **I/O Connector :** *50 pin male ribbon connector*
  20-pin male ribbon connector
- **I/O Cable Type :** *Ribbon stripline cable(Z_0 = 30Ω to 80Ω)*
- **Dimensions :** *95mm X 90mm*
- **Weight :** *200g*
- **Operating Temperature :** *0°C to 60°C*
- **Storage Temperature :** *-40°C to 100°C*
- **Humidity :** *0 to 90%, non-condensing*

1.5 Accessories Guide

- **AX751**
  Screw terminal board for all digital I/O connections. Shipped with 3.3 feet (1 meter) cable and 50-pin connector.

- **AX754**
  24-channel opto-isolated D/I panel for signal connection and conditioning with the AX10424. Shipped with 3.3 feet (1 meter) cable and 50-pin connector.

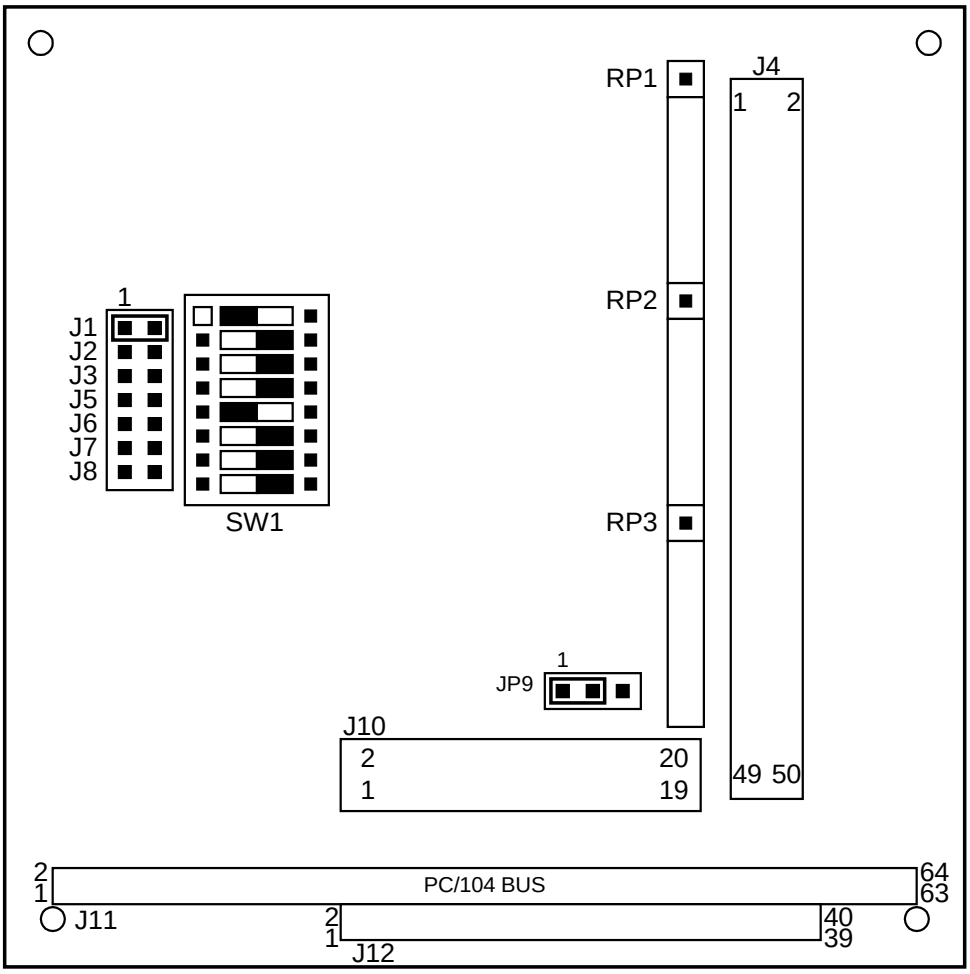
- **AX755**
  8-channel electromechanical single-pole, double-throw(SPDT) and 16-channel opto-isolated digital I/P panel which is compatible with the AX10424. Shipped with 3.3 feet (1 meter) cable and 50-pin connector.

- **AX756**
  24-channel electromechanical single-pole, double-throw(SPDT) which can be driven by the AX10424. Shipped with 3.3 feet (1 meter) cable and 50-pin connector.

Chapter 2
Module Configuration and Installation

2.1 Component Locator Diagram

The following figure shows the location of AX10424's components. All switch and jumper settings in this figure are the factory default setting.

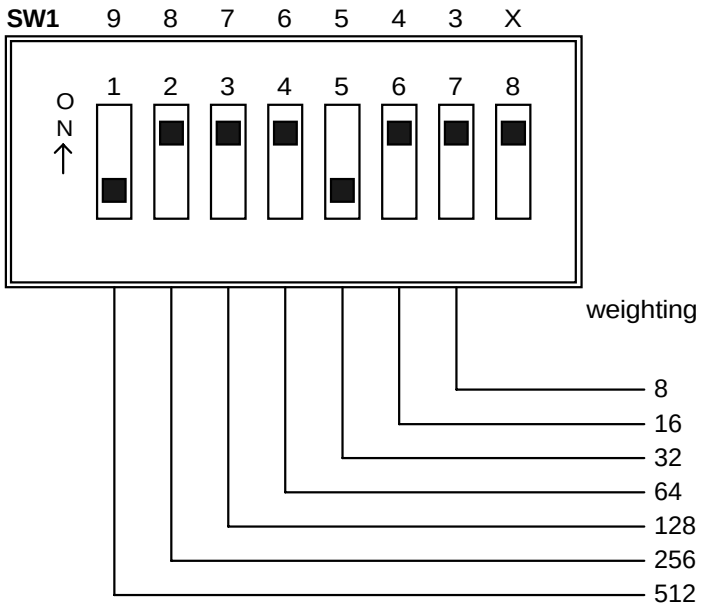


2.2 Base Address Switch

AX10424 occupies eight consecutive I/O port spaces. The I/O port addresses are set via a DIP switch labeled SW1. Set the DIP switch to correct address and avoid conflicting with other devices (refer to ***Appendix A*** for I/O port distribution). Valid addresses are from 200 Hex to 3F8 Hex. Following figure is the default setting where the base address is set to 220 Hex.

To set to appropriate base address, switch the individual switches into the ON or OFF position. Figure below shows the DIP switch default setting, 220 Hex, where switches 1 and 5 are moved to the OFF position while leaving all other switches in the ON position. A table for DIP switch setting is given in the following page.

Base Address Switch Setting



X : Not used.

Base Address = 512 + 32 = 544 (Decimal)
= 220 (Hexadecimal)

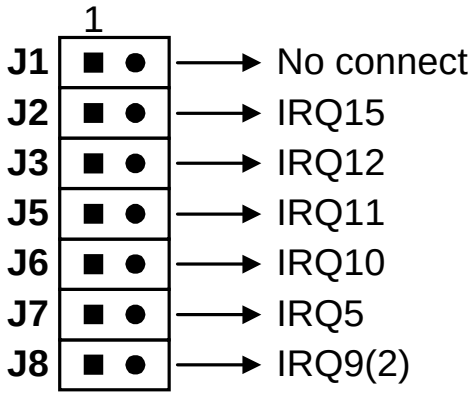
I/O Port Range	DIP Switch Position							
Hexadecimal	1	2	3	4	5	6	7	8
	A9	A8	A7	A6	A5	A4	A3	A2
200 – 207	1	0	0	0	0	0	0	X
208 – 20F	1	0	0	0	0	0	1	X
210 – 217	1	0	0	0	0	1	0	X
218 – 21F	1	0	0	0	0	1	1	X
220 – 227 (*)	1	0	0	0	1	0	0	X
.	.				.		.	
.	.				.		.	
300 – 307	1	1	0	0	0	0	0	X
.	.				.		.	
.	.				.		.	
3F0 – 3F7	1	1	1	1	1	1	0	X
3F8 – 3FF	1	1	1	1	1	1	1	X

NOTE *0 = ON, 1 = OFF, X = don't care*

(*) : Factory Default Setting

2.3 Interrupt Select Jumper

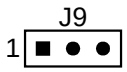
The AX10424 accept external inputs at INTE and INTP pins of J10 20-pin connector. These inputs are lead to any of six interrupt request lines (IRQ level 9(2), 5, 10, 11, 12, 15) by the following jumpers.

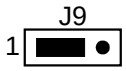
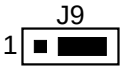


In factory jumper J1 is installed.

2.4 12V or Ground Selection

Pin 2 and Pin 4 of J4 (50-pin connector) can be set to output PC +12V or Ground by setting jumper J9. The J9 configuration is listed in below table.



J9 jumper configuration	 Factory default setting	
Pin 2 and 4 at J4 connector	Connected to Ground	Connected to +12V
J4 compatible	AX1416, AX1424, etc.	AX754, AX755, AX756, etc.

Jumpering PC +12V to J4 connector allows the AX10424 to provide +12V power for direct relay driving voltage or input pull high voltage. Note that when using the AX10424 with standard Opto-22 interface panel board, pins 1 and 2 of J9 jumper must be connected.

2.5 Connector Pin Assignment

All AX10424 DIO signals are built into a 50-pin connector labeled J4 whose pin assignments are shown below. Via this connector the AX10424 in compatible with AX751, AX754, AX755, AX756 accessory board or standard Opto-22 interface panel.

Name	Pin	Pin	Name	I/O Channel
Ground	50	49	+5V	-
Ground	48	47	PA 0	0
Ground	46	45	PA 1	1
Ground	44	43	PA 2	2
Ground	42	41	PA 3	3
Ground	40	39	PA 4	4
Ground	38	37	PA 5	5
Ground	36	35	PA 6	6
Ground	34	33	PA 7	7
Ground	32	31	PB 0	8
Ground	30	29	PB 1	9
Ground	28	27	PB 2	10
Ground	26	25	PB 3	11
Ground	24	23	PB 4	12
Ground	22	21	PB 5	13
Ground	20	19	PB 6	14
Ground	18	17	PB 7	15
Ground	16	15	PC 0	26
Ground	14	13	PC 1	17
Ground	12	11	PC 2	18
Ground	10	9	PC 3	19
Ground	8	7	PC 4	20
Ground	6	5	PC 5	21
(*)	4	3	PC 6	22
(*)	2	1	PC 7	23

NOTE *+5V : +5V PC power supply*

(*) : These pins can be connected to +12V PC power or Ground by jumpering J9. Refer to +12V or Ground Selection section

WARNING *As pin 2 and pin 4 of J4 can be connected to GND or +12V, by setting J9 jumper, thus when the AX10424 is connected to other card through this 50-pin connector, user must pay attention to the connector pin assignment (especially pins 2 and 4) of the corresponding card.*

All input or output lines of AX10424 counter/timer are built into J10 (20-pin connector). The J10 connector pin assignments are as follows:

Name	Pin	Pin	Name
CLK0	1	2	+12V
G0	3	4	GND
OUT0	5	6	GND
CLK1	7	8	GND
G1	9	10	10MHz
OUT1	11	12	GND
CLK2	13	14	INTP
G2	15	16	INTE
OUT2	17	18	GND
N/C	19	20	+5V

CLK0 – CLK2 : *Clock input to 8254 counter 0 through 2*

+12V : *+12V PC power*

G0 – G2 : *Gate control input to 8254 counter 0 through 2*

GND : *Ground*

OUT0 – OUT2 : *Output from 8254 counter 0 through 2*

10MHz : *10MHz frequency output*

INTP *Interrupt trigger input*

INTE : *Interrupt enable input*

N/C : *No connect*

+5V : *+5V PC power*

2.6 Resistor Pack

As mentioned before the 8-bit port digital I/O lines can be configured as input or output port (refer to ***Chapter 3***). Initially the digital I/O lines are left floating. When any of these ports is set to input port, user is suggested to pull high it's input lines by installing RP(s). Onboard there are 3 reserved spaces, marked as RP1 – RP3 (refer to table below, the RP is approximately 4.7K).

If a port is configured as output lines, just leave the corresponding RP unoccupied.

If J4 is connected to AX1416 and AX1424, the RP should be installed to prevent power-on floating phenomenon. This floating may cause SSR to action (switch on).

DIO Lines	RP
Port A	RP3
Port B	RP2
Port C	RP1

NOTE *In some situations, i.e. environment ground is not stable, the digital output reset frequently. User is suggested to isolate system circuitry from external signals. Let the external signal to go through AX754 (24 channel opto-isolated D/O panel) or AX755 (8 channel relay output and 16 channel opto-isolated D/I panel) or AX756 (24 channel relay output) before reaching the system circuitry.*

2.7 Hardware Description

PC/104 module can be of two bus types, 8 bit and 16 bit. These correspond to the PC and PC/AT buses, respectively. The detailed mechanical dimensions of these two PC/104 bus types are provided in ***Appendix E PC/104 Mechanical Specification***.

Basically the AX10424 belongs to 16 bit bus option which is designed only to by pass PC/AT bus signal in order to compatible to PC/AT type PC/104 module. The AX10424 use only IRQ lines on J12 40-pin connector. If this module is going to plug onto PC type PC/104 bus, do not use IRQ line above 10.

Besides bus option, there are stackthrough and non-stackthrough difference. The stackthrough version provides a self-stacking PC bus. It can be placed any where in a multi-module stack. The non-stackthrough version offers minimum thickness, by omitting bus stackthrough pins. It must be positioned at one end of a stack.

For convenience, the AX10424 is equipped with stackthrough version only.

NOTE *For safety, you are suggested to cut bus stackthrough pins of the last module on condition; that you are sure you won't add/plug any module to the module stack in the future.)*

2.8 Hardware Installation

The AX10424 PC/104 module is shipped with protective electrostatic cover. When unpacking, touching the module electrostatically shielded packaging with the metal frame of your computer to discharge the accumulated static electricity prior to touching the module.

Following description summarizes the procedure for installing the AX10424:

WARNING *Turn off the PC and all accessories connected to the PC whenever installing or removing any peripheral board including the AX10424 module.*

Installation Procedures:

1. Turn off the system power.
2. Unplug all power cords.
3. Remove the case cover if necessary.
4. Remove the top module if it is a non-stackthrough module.
5. Put the AX10424 module in line with the top present module as described in ***Appendix E PC/104 Mechanical Specification***.
6. Install four spacers if necessary.
7. Connect cable to J10 if necessary.
8. Crush between the modules until inside distance is SPACER's height (0.6"). Restore all the screws.
9. Repeat step 6 until all modules are set into position.
10. Connect cable (J4) to AX10424 if necessary.
11. Replace the case cover and connect all the necessary cables.
12. Turn on the system power.

Chapter 3
Register Structure and Format

3.1 AX10424 I/O Address Map

This chapter describes each AX10424 register in terms of function, address, bit structure and bit function. Each register is easy to read and write to by using direct I/O instructions of whatever application languages.

AX10424 uses 8 consecutive addresses in I/O space as follows (R = Read, W = Write):

Location	Function	Type
Base Address +0	Counter 0	R/W
Base Address +1	Counter 1	R/W
Base Address +2	Counter 2	R/W
Base Address +3	Control Word	W
Base Address +4	Port A	R/W
Base Address +5	Port B	R/W
Base Address +6	Port C	R/W
Base Address +7	Control Register	W

3.2 8254 Counter Data and Control Registers

- **Counter 0 Data Register (Base +0, R/W)**

base	7	6	5	4	3	2	1	0
+0	B7	B6	B5	B4	B3	B2	B1	B0

- **Counter 1 Data Register (Base +1, R/W)**

base	7	6	5	4	3	2	1	0
+1	B7	B6	B5	B4	B3	B2	B1	B0

- **Counter 2 Data Register (Base +2, R/W)**

base	7	6	5	4	3	2	1	0
+2	B7	B6	B5	B4	B3	B2	B1	B0

- **Counter Word Register (Base +3, R/W)**

base	7	6	5	4	3	2	1	0
+3	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

- **Where SC-Select Counter**

SC1	SC0	Description
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-back

- **Where RW – Read/Write**

RW1	RW0	Description
0	0	Counter latch command
0	1	R/W LSB only
1	0	R/W MSB only
1	1	R/W LSB first, then MSB

- **Where M – Mode**

M2	M1	M0	Description
0	0	0	Mode 0 : Pulse on terminal count
0	0	1	Mode 1 : Programmable one-shot
X	1	0	Mode 2 : Rate generate
X	1	1	Mode 3 : Square wave mode
1	0	0	Mode 4 : Software triggered mode
1	0	1	Mode 5 : Hardware triggered strobe

- **BCD – Binary Coded Decimal:**

BCD	Description
0	Binary counter 16-bit
1	Binary coded decimal (BCD) counter (4 decodes)

NOTE *This module uses 8254 integrate chip for its programmable counter/timer channels. Refer to* ***Appendix D Programming 8254 Counter/Timer*** *or the 8254 Data Book for detailed information.*

3.3 Digital I/O Registers

The 24 digital I/O lines of AX10424 are arranged into one group. This group emulates 8255 PPI chip mode 0 and is further divided into three ports; Port A, Port B and Port C.

The AX10424 is programmable through the configuration registers. By writing to control registers, the I/O direction of each port may be specified. If a port is configured as a write (output) port, the data drivers will drive the data value to the corresponding port. If a port is configured as a read (input) port, the data value on corresponding port will be sent to the digital I/O lines.

Only port C is different from the other two ports, that is Port C consists of two 4-bit ports, Port C-upper and Port C-lower, which can separately be configured as input or output port.

- **Port A Data Register (Base +4, R/W)**

base	7	6	5	4	3	2	1	0
+4	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

- **Port B Data Register (Base +5, R/W)**

base	7	6	5	4	3	2	1	0
+5	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

- **Port C Data Register (Base +6, R/W)**

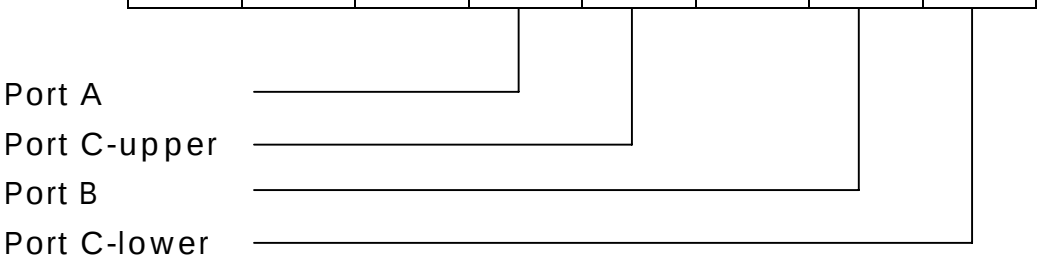
base	7	6	5	4	3	2	1	0
+6	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

PC0 – PC3 : Port C-lower Byte

PC4 – PC7 : Port C-upper Byte

- **Control Register (Base +7, W)**

base	7	6	5	4	3	2	1	0
+7	X	X	X	D4	D3	X	D1	D0



Note *PA0 – PA7, PB0 – PB7 and PC0 – PC7 bits are associated to pins at J4 connector.*

X = don't care

For D0, D1, D3, D4 : 1 → Input, 0 → Output

Chapter 4
Programming

AX10424 provides 24 bit digital I/O which are divided into three 8-bit ports (A, B and C). Port C is divided into two 4-bit nibbles; Port C-upper and C-lower. The I/O direction of the ports (Port A, B, C-upper and C-lower) can be determined by programming to the control register.

4.1 Programming Examples

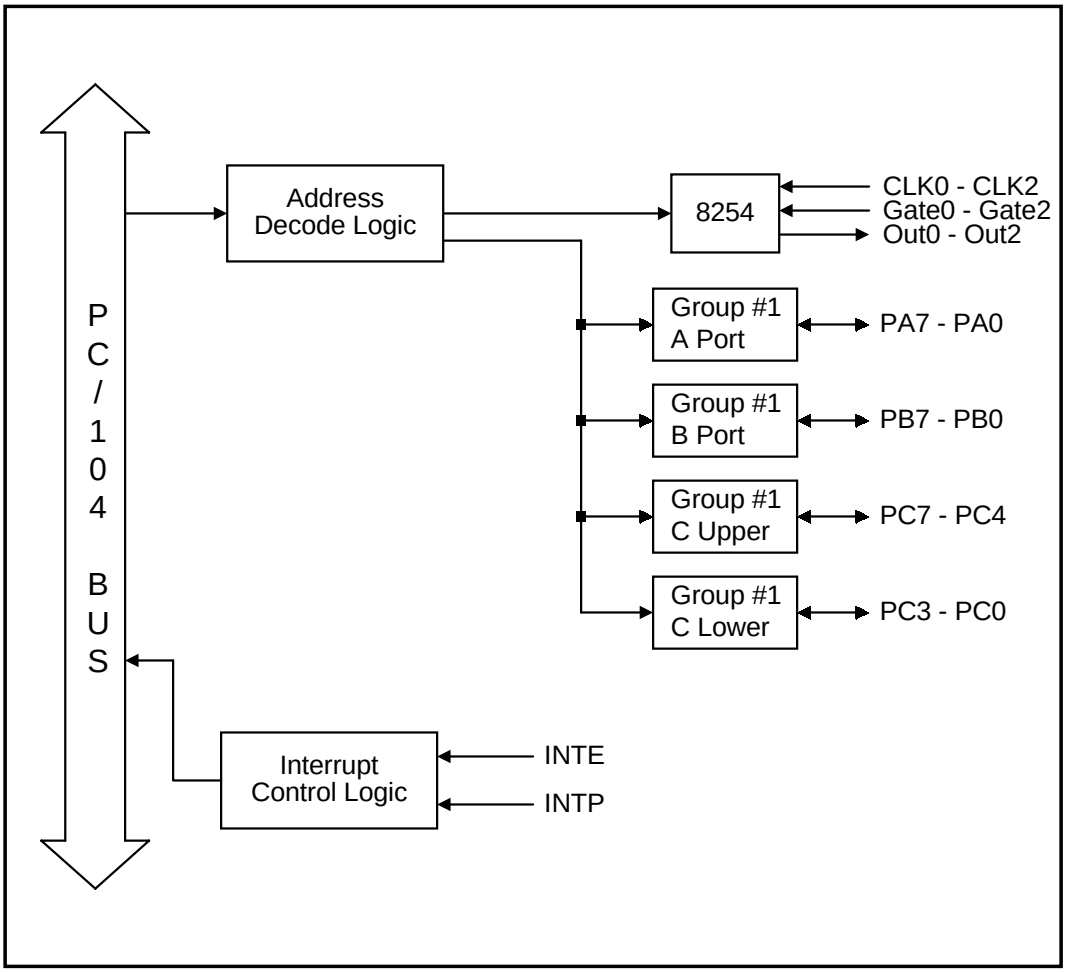
The following BASIC program configures Port A and B as input port (install corresponding RP's if necessary), Port C as output. An increasing pattern is sent to Port C. It is expected that user will connect both Port A and Port B to Port C before running this program.

```
10 CLS
20 PORT% = &H220          ' REM Base Address
30 OUT PORT %+7, &H92     ' REM Port A, B: input, C: output
40 FOR C=0 to 255         ' REM decimal value from 00 to FF
50 OUT PORT %+6, C        ' REM output data to Port C
60 A = INP (PORT%+4)      ' REM read data on Port A
70 B = INP (PORT%+5)      ' REM read data on Port B
80 PRINT A, B, C          ' REM check data versus Port A and B
90 NEXT C
100 END
```

Appendix A
PC I/O Port Mapping

I/O Port Address Range	Function
000 – 1FF	PC reserved
200 – 20F	Game controller (Joystick)
278 – 27F	Second parallel print (LPT2)
2E1	GPIB controller
2F8 – 2FF	Second serial port (COM2)
320 – 32F	Fixed disk (XT)
378 – 37F	Primary parallel print port (LPT1)
380 – 38F	SDLC communication port
3B0 – 3BF	Monochrome adapter/printer
3C0 – 3CF	EGA, reserved
3D0 – 3DF	Color/graphics adapter
3F0 – 3F7	Floppy disk controller
3F8 – 3FF	Primary serial port (COM1)

Appendix B
Block Diagram

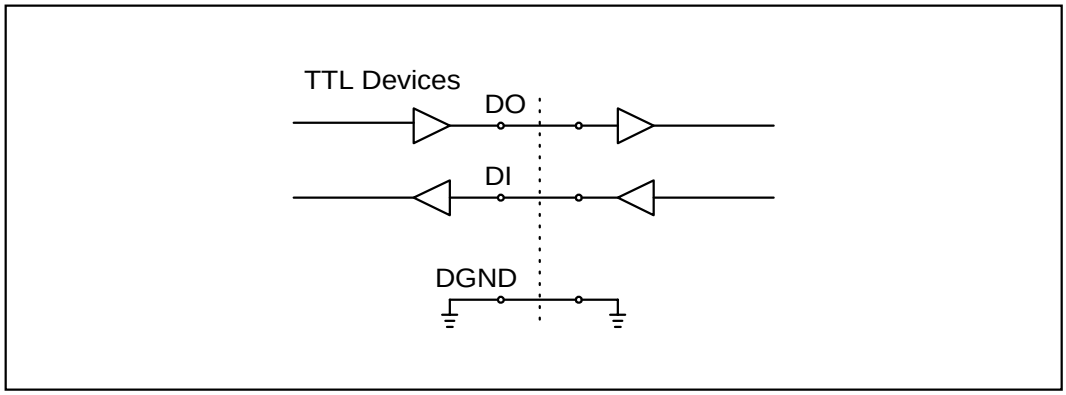


Appendix C
Technical Reference

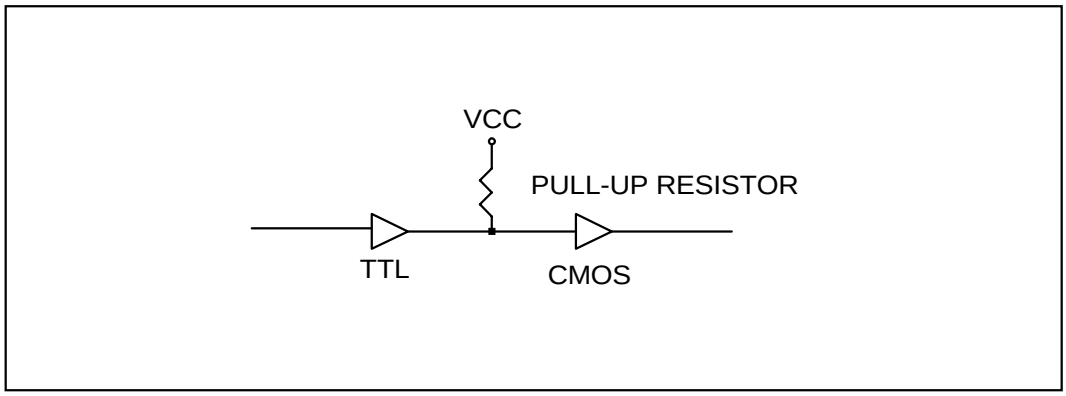
General Usage of Digital Input and Output

Digital signals are usually used for detecting logical status or controlling devices, a brief description is given below. TTL level signals are developed by most DAS systems.

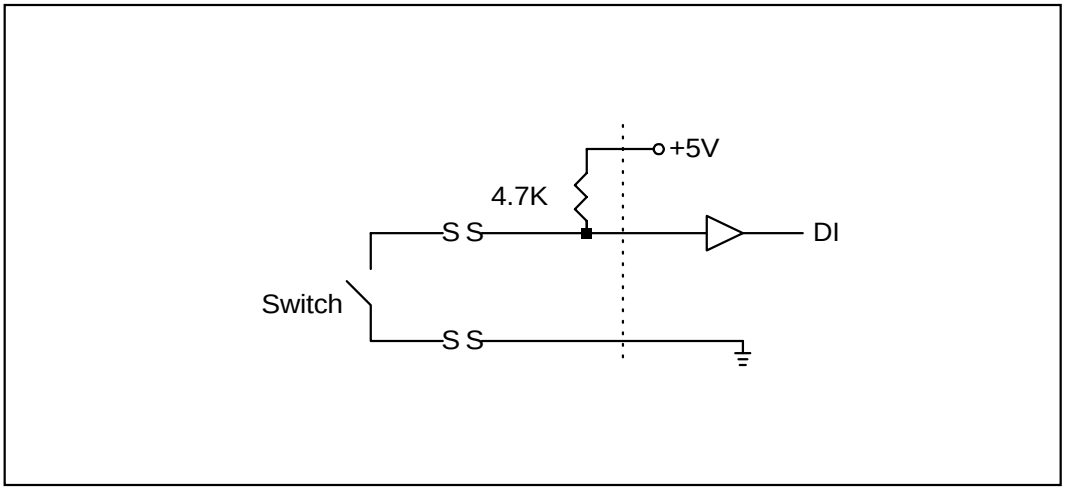
- **TTL or LSTTL Level I/O Connections**



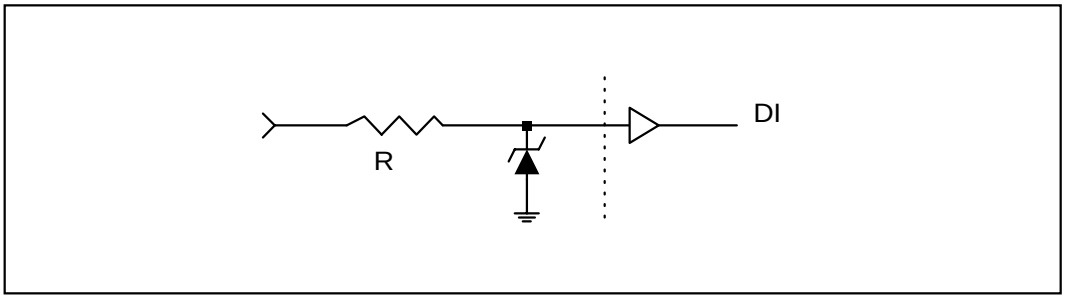
Connection with CMOS Device – Use a pull-up resistor if you wish to interface to CMOS devices. This will raise the logic high output level from its minimum TTL level of 2.4V to +5V suitable for CMOS interface.



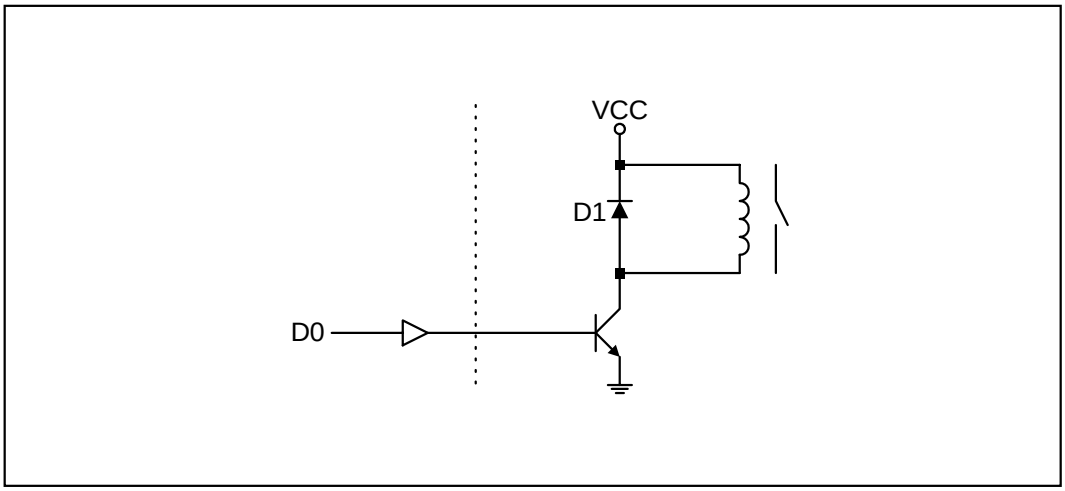
Digital Input for Open/Short Switch Detection – A pull-up resistor must be connected, especially at long distance wiring, to ensure logic high input level.



■ Digital Input for Large Signal

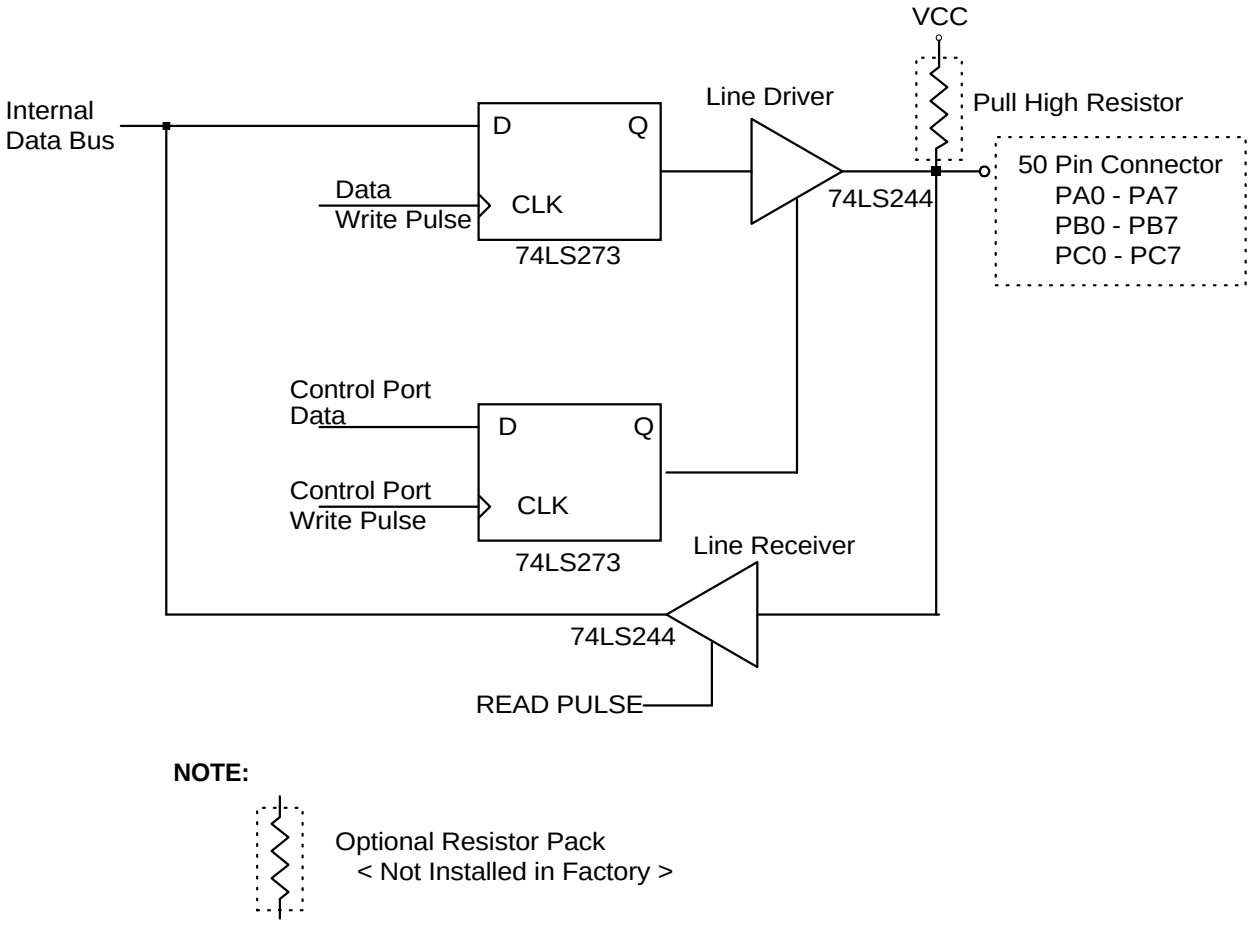


Digital Output for Relay Driving - The D1 diode is added to protect the IC driver against the inductive "kickback" from the relay coil.



AX10424 Port A, B and C Basic Definition

1. **Equivalent ckt of port A, B and C.**



2. **Any port is programmable to input or output.**
3. **Outputs are drived by 74LS244 and latched by 74LS273.**
4. **Inputs are received by 74LS244 but not latched.**
5. **All inputs and outputs are buffered by standard line drivers and line receivers.**
6. **The initial state and default setting of port A, B and C are tri-state.**

Appendix D
Programming 8254 Counter/Timer

Introduction

AXIOMTEK's AX10424 module uses INTEL 8254 which consist of three independently programmable 16-bit counters for its timing function. Each counter can be programmed to be divided by number within the range of 2 – 65535. The 8254 is suitable for:

- **Event counter**
- **Delay time generator**
- **Programmable one-shot**
- **Square wave generator**

For detail information, user should refer to the 8254 Programmable Interval Timer data sheet.

Counter Read/Write and Control Register

There are 4 registers needed to program 8254 Timer/Counter, including three Read/Write and one Control registers as follows:

Base +0 through Base +3

Base +0	Counter 0	Read/Write register
Base +1	Counter 1	Read/Write register
Base +2	Counter 2	Read/Write register
Base +3	Control word register	

Read/Write register is used to load divisor to select counter, or Read count from selected counter.

Control register is used to determine counter's operation.

Control Word Format

Address base +3

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

- **SC – Select Counter:**

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See read operations)

- **M – Mode:**

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

- **RW – Read/Write:**

RW1	RW0	
0	0	Counter Latch Command (see read operations)
0	1	Read/Write least significant byte only
	0	Read/Write most significant byte
1	1	Read/Write least significant byte first, then most significant byte.

- **BCD – Binary Coded Decimal:**

0	Binary Counter 16-bits
1	Binary Coded ecimal (BCD) (4 Decades)

NOTE *Don't care bits (X) should be 0 to insure compatibility with future products.*

Read-Back Command

The read-back command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in the preceeding page. The command applies to the counters selected by setting their corresponding bits D3, D2, D1 = 1.

Base Address +3

D7	D6	D5	D4	D3	D2	D1	D0
1	1	COUNT	STATUS	CNT 2	CNT 1	CNT 0	0

D5 : 0 = Latch count of selected Counter (s)

D4 : 0 = Latch status of selected Counter (s)

D3 : 1 = Select Counter 2

D2 : 1 = Select Counter 1

D1 : 1 = Select Counter 0

D0 : Reserved for future expansion, Must be 0

Here is an example for read-back command:

Command								Description	Result
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read-back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read-back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read-back status of Counter 2 and 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read-back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read-back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read-back status of Counter 1	Command ignored, status already latched for Counter 1

Counter Operation Mode

Mode 0 : Interrupt on Terminal Count

Mode 0 is typical used for event counting. After the Control Word is written, OUT is initially low, and will remain low until Counter reaches Zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

Gate = 1 enables counting; GATE = 0 disables counting.

GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue form the new count.

If a two-byte count is written, the following happens:

- **Writing the first byte disables counting. Out is set low immediately (no clock pulse required).**
- **Writing the second byte allows the new count to be loaded on next CLK pulse.**

Mode 1 : Hardware Retirggerable One-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-short pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-short pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

Mode 2 : Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. Out will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT the goes high again, the Counter reloads the initial count and the process is repeated Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulse after the initial count is written. This allows the Counter to be synchronized by software also.

Mode 3 : Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initial be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Mode 3 is implemented as follows:

- **Even Counts:**

  OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

- **ODD Counts:**

  OUT is initially high. The initial count is loaded on one CLK pulse, decremented by one on the next CLK pulse, and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the Counter is reloaded with the initial count. The count is decremented by three on the next CLK pulse, and then by two on succeeding CLK pulses. When the count expires, OUT goes high again repeated indefinitely. So for odd counts, OUT will be high for (N + 1) /2 counts and low for (N – 1)/2 counts.

Mode 4 : Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse then go high again. The counting sequence is "Triggered" by writing the initial count.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loading on the next CLK pulse and counting will continue form the new count.

If a two-byte count is written, the following happens:

- **Writing the first byte has no effect on counting.**
- **Writing the second byte allows the new count to be loaded on the next CLK pulse.**

This allows the sequence to be "retriggered" by software OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5 : Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

Programming Counter/Timer

Programming Sequence:

1. **Writing control word to select counter and determine operation.**
2. **Program selected counter's LSB of R/W register.**
3. **Program selected counter's MSB of R/W register.**

Address Base +		Address Base +	
Control Word - Counter 0	3	Control Word - Counter 2	3
LSB of count - Counter 0	0	Control Word - Counter 1	3
MSB of count - Counter 0	0	Control Word - Counter 0	3
Control Word - Counter 1	3	LSB of count - Counter 2	2
LSB of count - Counter 1	1	MSB of count - Counter 2	2
MSB of count - Counter 1	1	LSB of count - Counter 1	1
Control Word - Counter 2	3	MSB of count - Counter 1	1
LSB of count - Counter 2	2	LSB of count - Counter 0	0
MSB of count - Counter 2	2	MSB of count - Counter 0	0
Control Word - Counter 0	3	Control Word - Counter 1	3
Control Word - Counter 1	3	Control Word - Counter 0	3
Control Word - Counter 2	3	LSB of count - Counter 1	1
LSB of count - Counter 2	2	Control Word - Counter 2	3
LSB of count - Counter 1	1	LSB of count - Counter 0	0
LSB of count - Counter 0	0	MSB of count - Counter 1	1
LSB of count - Counter 0	0	LSB of count - Counter 2	2
MSB of count - Counter 1	1	MSB of count - Counter 0	0
MSB of count - Counter 2	2	MSB of count - Counter 2	2

NOTE *In all four examples, all counters are programmed to Read/Write two-byte count is. These are only four of many possible programming sequences.*

Simple programming examples written in BASIC are given as follows:

■ Example 1 Program counter 0 as rate generator

```
10  Divisor% = 100
20  LSB% = Divisor% MOD 256
30  MSB% = Divisor%\256
40  Base% = &H220
50  OUT Base%+3, &H34          ' Counter 0: rate generator
60  OUT Base%+0, LSB%          ' Write low byte to counter 0
70  OUT Base%+0, MSB%          ' Write high byte to counter 0
```

■ Example 2 Read count of counter 0

```
10  Base% = &H220
20  OUT Base%+3, 0             ' Latch counter 0
30  LSB%=inp(Base%+0)          ' Read low byte from counter 0
40  MSB%=inp(Base%+0)          ' Read high byte from counter 0
50  Count%=LSB%+MSB%*256       ' Read count from counter 0
```

Appendix E
PC/104 Mechanical Specification

PC/104 General Description

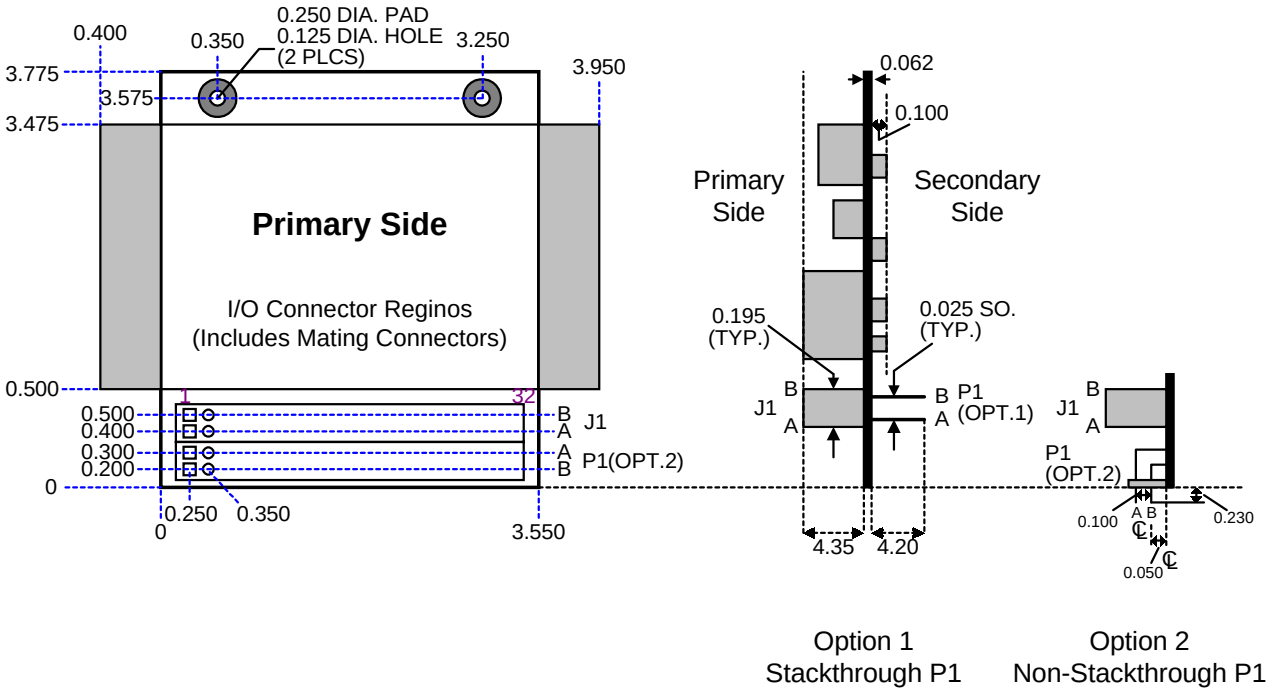
While the PC and PC/AT architectures have become extremely popular in both general purpose (desktop) and dedicated (non-desktop) applications, its use in embedded microcomputer applications has been limited due to the large size of standard PC and PC/AT motherboards and expansion cards.

This document supplies the mechanical and electrical specifications for a compact version of the PC/AT bus, optimized for the unique requirements of embedded systems applications. The specification is herein referred to as "PC/104", based on the 104 signal contacts on the two bus connectors (64 pins on J11 plus 40 pins on J12).

Module Dimensions

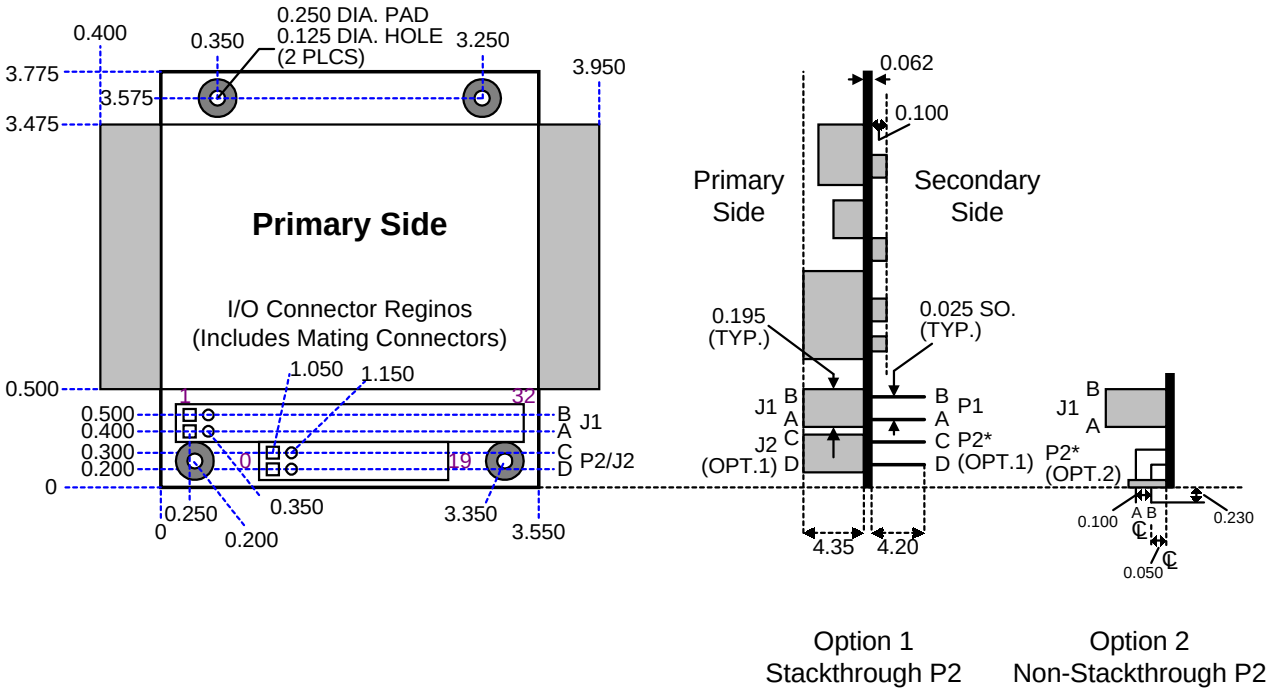
PC/104 modules can be of two bus types, 8-bit and 16-bit. These correspond to the PC and PC/AT buses, respectively.

■ PC/104 8-Bit Module Dimensions



NOTE *Dimensions are in inches ±0.05.*

■ PC/104 16-Bit Module Dimensions



NOTE *Dimensions are in inches ±0.05.*
Difference in P2 OPT.1 and OPT.2 pin orientations.

Typical Module Stack

The following figure illustrates a typical module stack of 8-bit modules, and shows the use of the "stack-through" and "non-stackthrough" J11 bus connector options.