Functional Description (Continued)

3.4.3.4 General Purpose I/O Pins

The CS5530A provides up to eight GPIO (general purpose I/O) pins. Five of the pins (GPIO[7:4] and GPIO1) have alternate functions. Table 3-31 shows the bits used for GPIO pin function selection.

Each GPIO pin can be configured as an input or output. GPIO[7:0] can be independently configured to act as edge-sensitive SMI events. Each pin can be enabled and configured to be either positive-edge sensitive or negative-edge sensitive. These pins then cause an SMI to be generated when an appropriate edge condition is detected. The power management status registers indicate that a GPIO external SMI event has occurred.

The GPIO Pin Direction Register 1 (F0 Index 90h) selects whether the GPIO pin is an input or output. The GPIO Pin Data Register 1 (F0 Index 91h) contains the direct values of the GPIO pins. Write operations are valid only for bits defined as outputs. Reads from this register read the last written value if the pin is an output.

GPIO Control Register 1 (F0 Index 92h) configures the operation of the GPIO pins for their various alternate functions. Bits [5:3] set the edge sensitivity for generating an SMI on the GPIO[2:0] (input) pins respectively. Bits [2:0] enable the generation of an SMI. Bit 6 enables GPIO6 to act as the lid switch input. Bit 7 determines which edge transition will cause General Purpose Timer 2 (F0 Index 8Ah) to reload.

Table 3-32 shows the bit formats for the GPIO pin configuration and control registers.

Table 3-31. GPIO Pin Function Selection

Bit	Description
F0 Index 43h	**USB Shadow Register (R/W)** — **Reset Value = 03h**
6	**Enable SA20:** Pin AD22 configuration: 0 = GPIO4; 1 = SA20. If F0 Index 43h bit 6 or bit 2 is set to 1, then pin AD22 = SA20.
2	**Enable SA[23:20]:** Pins AF23, AE23, AC21, and AD22 configuration: 0 = GPIO[7:4]; 1 = SA[23:20]. If F0 Index 43h bit 6 or bit 2 is set to 1, then pin AD22 = SA20.
F3BAR+Memory Offset 08h-0Bh	**Codec Status Register (R/W)** — **Reset Value = 00000000h**
21	**Enable SDATA_IN2:** Pin AE24 functions as: 0 = GPIO1; 1 = SDATA_IN2. For this pin to function as SDATA_IN2, it must first be configured as an input (F0 Index 90h[1] = 0).

Table 3-32. GPIO Pin Configuration/Control Registers

Bit	Description
F0 Index 90h	**GPIO Pin Direction Register 1 (R/W)** — **Reset Value = 00h**
7	**GPIO7 Direction:** Selects if GPIO7 is an input or output: 0 = Input; 1 = Output.
6	**GPIO6 Direction:** Selects if GPIO6 is an input or output: 0 = Input; 1 = Output.
5	**GPIO5 Direction:** Selects if GPIO5 is an input or output: 0 = Input; 1 = Output.
4	**GPIO4 Direction:** Selects if GPIO4 is an input or output: 0 = Input; 1 = Output.
3	**GPIO3 Direction:** Selects if GPIO3 is an input or output: 0 = Input; 1 = Output.
2	**GPIO2 Direction:** Selects if GPIO2 is an input or output: 0 = Input; 1 = Output.
1	**GPIO1 Direction:** Selects if GPIO1 is an input or output: 0 = Input; 1 = Output.
0	**GPIO0 Direction:** Selects if GPIO0 is an input or output: 0 = Input; 1 = Output.
Note: Several of these pins have specific alternate functions. The direction configured here must be consistent with the pins' use as the alternate function.	
F0 Index 91h	**GPIO Pin Data Register 1 (R/W)** — **Reset Value = 00h**
7	**GPIO7 Data:** Reflects the level of GPIO7: 0 = Low; 1 = High.
6	**GPIO6 Data:** Reflects the level of GPIO6: 0 = Low; 1 = High.
5	**GPIO5 Data:** Reflects the level of GPIO5: 0 = Low; 1 = High.
4	**GPIO4 Data:** Reflects the level of GPIO4: 0 = Low; 1 = High.
3	**GPIO3 Data:** Reflects the level of GPIO3: 0 = Low; 1 = High.
2	**GPIO2 Data:** Reflects the level of GPIO2: 0 = Low; 1 = High.
1	**GPIO1 Data:** Reflects the level of GPIO1: 0 = Low; 1 = High.
0	**GPIO0 Data:** Reflects the level of GPIO0: 0 = Low; 1 = High.
Note: This register contains the direct values of GPIO[7:0] pins. Write operations are valid only for bits defined as output. Reads from this register will read the last written value if the pin is an output. The pins are configured as inputs or outputs in F0 Index 90h.	

Functional Description (Continued)

Table 3-32. GPIO Pin Configuration/Control Registers (Continued)

Bit	Description
F0 Index 92h	**GPIO Control Register 1 (R/W)** — **Reset Value = 00h**
7	**GPIO7 Edge Sense for Reload of General Purpose Timer 2:** Selects which edge transition of GPIO7 causes GP Timer 2 to reload. 0 = Rising; 1 = Falling (Note 2).
6	**GPIO6 Enabled as Lid Switch:** Allow GPIO6 to act as the lid switch input. 0 = GPIO6; 1 = Lid switch. When enabled, every transition of the GPIO6 pin causes the lid switch status to toggle and generate an SMI. The top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 87h/F7h[3]. If GPIO6 is enabled as the lid switch, F0 Index 87h/F7h[4] reports the current status of the lid's position.
5	**GPIO2 Edge Sense for SMI:** Selects which edge transition of the GPIO2 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 2 must be set to enable this bit.
4	**GPIO1 Edge Sense for SMI:** Selects which edge transition of the GPIO1 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 1 must be set to enable this bit.
3	**GPIO0 Edge Sense for SMI:** Selects which edge transition of the GPIO0 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 1 must be set to enable this bit.
2	**Enable GPIO2 as an External SMI Source:** Allow GPIO2 to be an external SMI source and generate an SMI on either a rising or falling edge transition (depends upon setting of bit 5). 0 = Disable; 1 = Enable (Note 3). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 87h/F7h[7].
1	**Enable GPIO1 as an External SMI Source:** Allow GPIO1 to be an external SMI source and generate an SMI on either a rising- or falling-edge transition (depends upon setting of bit 4). 0 = Disable; 1 = Enable (Note 3). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 87h/F7h[6].
0	**Enable GPIO0 as an External SMI Source:** Allow GPIO0 to be an external SMI source and generate an SMI on either a rising or falling edge transition (depends upon setting of bit 3). 0 = Disable; 1 = Enable (Note 3) Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 87h/F7h[5].
Notes: 1) For any of the above bits to function properly, the respective GPIO pin must be configured as an input (F0 Index 90h). 2) GPIO7 can generate an SMI (F0 Index 97h[3]) or re-trigger General Purpose Timer 2 (F0 Index 8Bh[2]) or both. 3) If GPIO[2:0] are enabled as external SMI sources, they are the only GPIOs that can be used as SMI sources to wake-up the system from Suspend when the clocks are stopped.	
F0 Index 97h	**GPIO Control Register 2 (R/W)** — **Reset Value = 00h**
7	**GPIO7 Edge Sense for SMI:** Selects which edge transition of the GPIO7 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 3 must be set to enable this bit.
6	**GPIO5 Edge Sense for SMI:** Selects which edge transition of the GPIO5 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 2 must be set to enable this bit.
5	**GPIO4 Edge Sense for SMI:** Selects which edge transition of the GPIO4 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 1 must be set to enable this bit.
4	**GPIO3 Edge Sense for SMI:** Selects which edge transition of the GPIO3 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 0 must be set to enable this bit.
3	**Enable GPIO7 as an External SMI Source:** Allow GPIO7 to be an external SMI source and to generate an SMI on either a rising or falling edge transition (depends upon setting of bit 7). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[3].
2	**Enable GPIO5 as an External SMI Source:** Allow GPIO5 to be an external SMI source and to generate an SMI on either a rising or falling edge transition (depends upon setting of bit 6). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[2].
1	**Enable GPIO4 as an External SMI Source:** Allow GPIO4 to be an external SMI source and to generate an SMI on either a rising- or falling-edge transition (depends upon setting of bit 5). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[1].

Functional Description (Continued)

Table 3-32. GPIO Pin Configuration/Control Registers (Continued)

Bit	Description
0	**Enable GPIO3 as an External SMI Source:** Allow GPIO3 to be an external SMI source and to generate an SMI on either a rising or falling edge transition (depends upon setting of bit 4) 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[0].
Note: For any of the above bits to function properly, the respective GPIO pin must be configured as an input (F0 Index 90h).	